

(10) **Patent No.:** US 9,425,190 B2
(45) **Date of Patent:** *Aug. 23, 2016

- (58) **Field of Classification Search**
CPC G11C 16/10; G11C 5/06
USPC 365/72, 185.24
See application file for complete search history.

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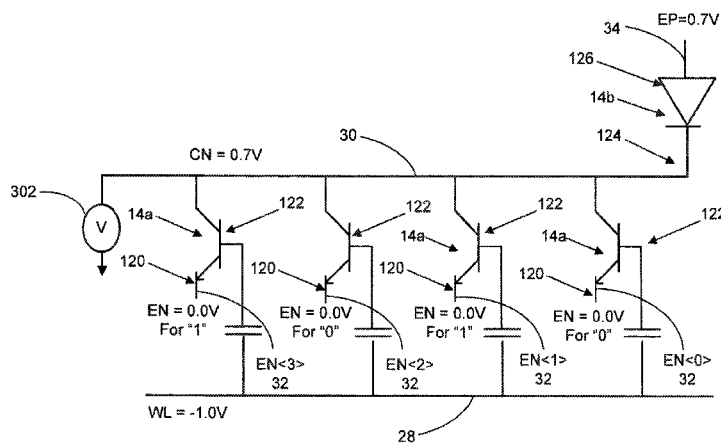
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- (57) **ABSTRACT**

- Techniques for providing a direct injection semiconductor memory device are disclosed. In one particular exemplary embodiment, the techniques may be realized as a method for biasing a direct injection semiconductor memory device. The method may comprise applying a first voltage potential to a first N-doped region via a bit line and applying a second voltage potential to a second N-doped region via a source line. The method may also comprise applying a third voltage potential to a word line, wherein the word line is spaced apart from and capacitively coupled to a body region that is electrically floating and disposed between the first N-doped region and the second N-doped region. The method may further comprise applying a fourth voltage potential to a P-type substrate via a carrier injection line.

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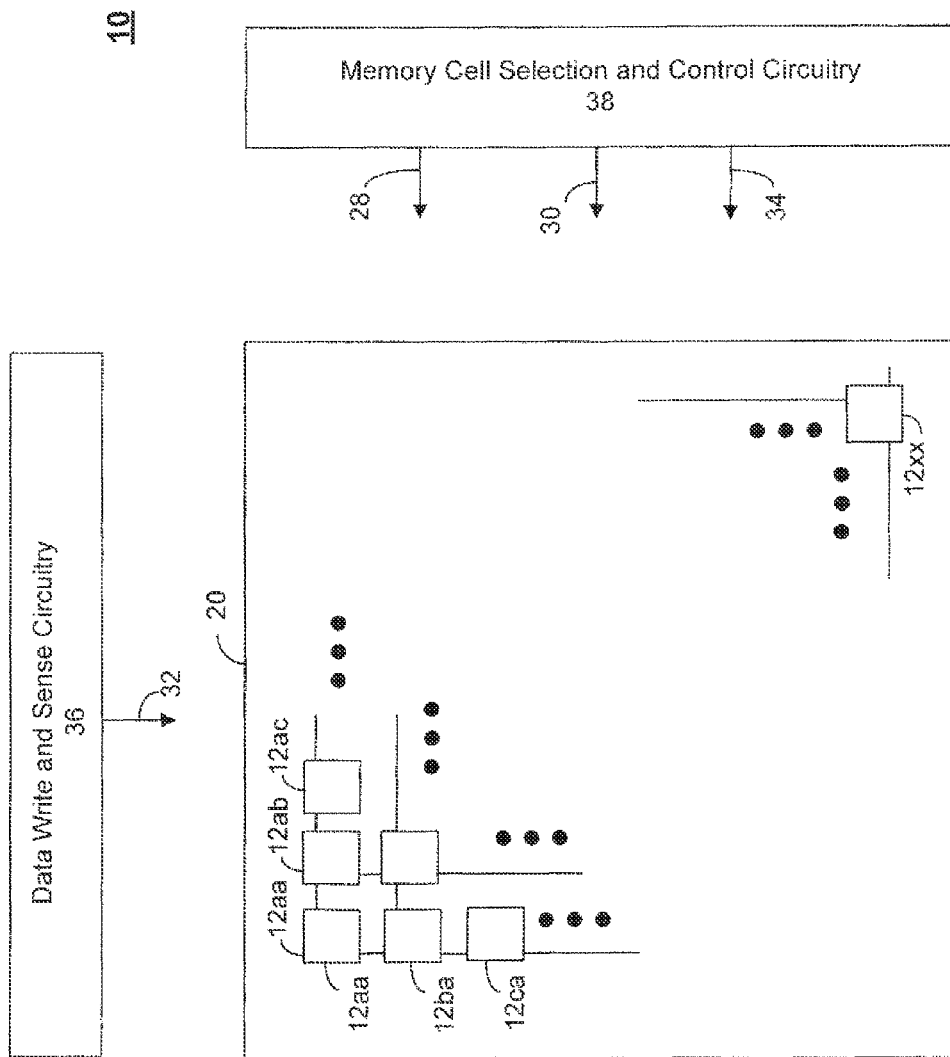


FIGURE 1

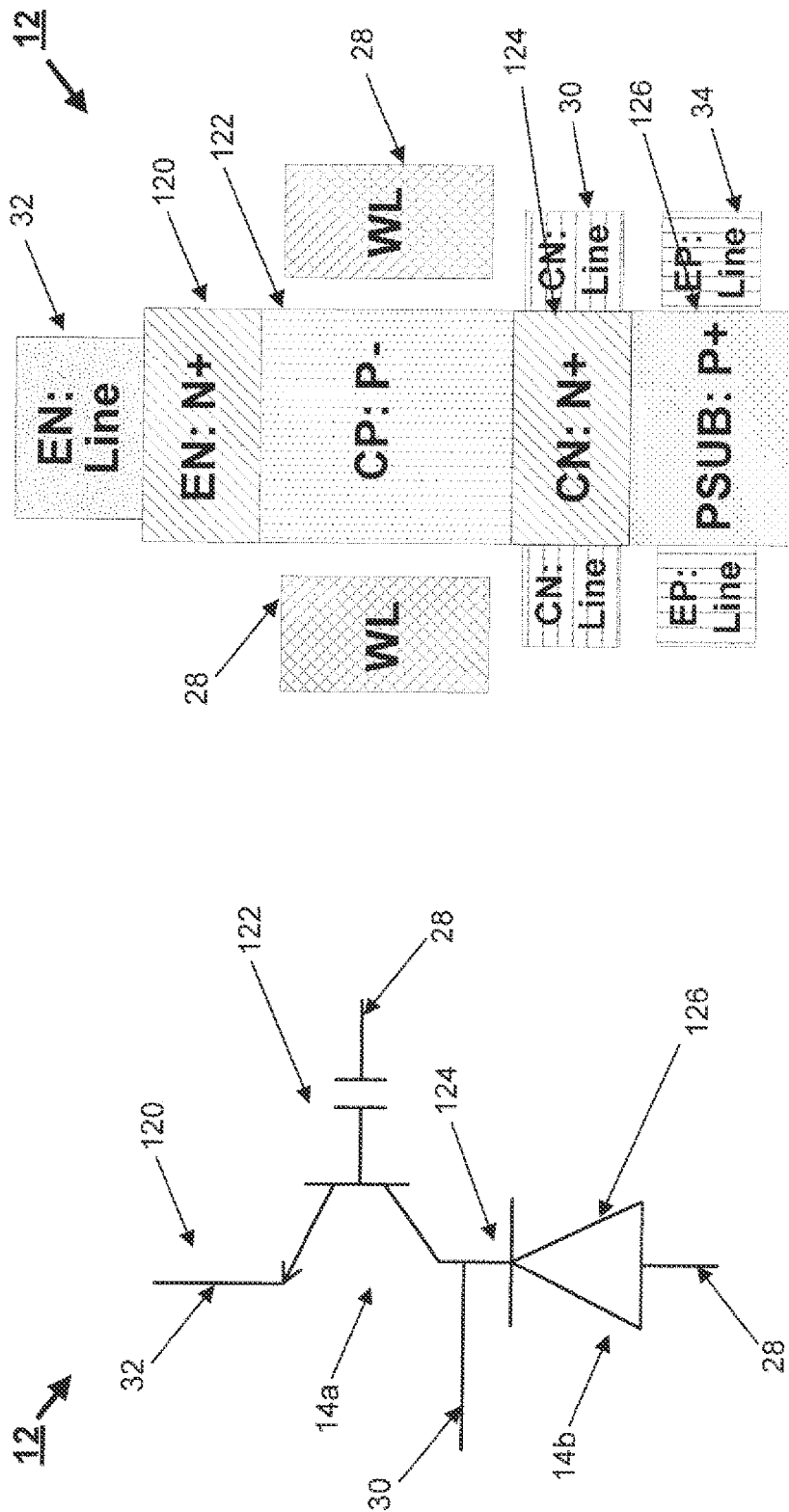
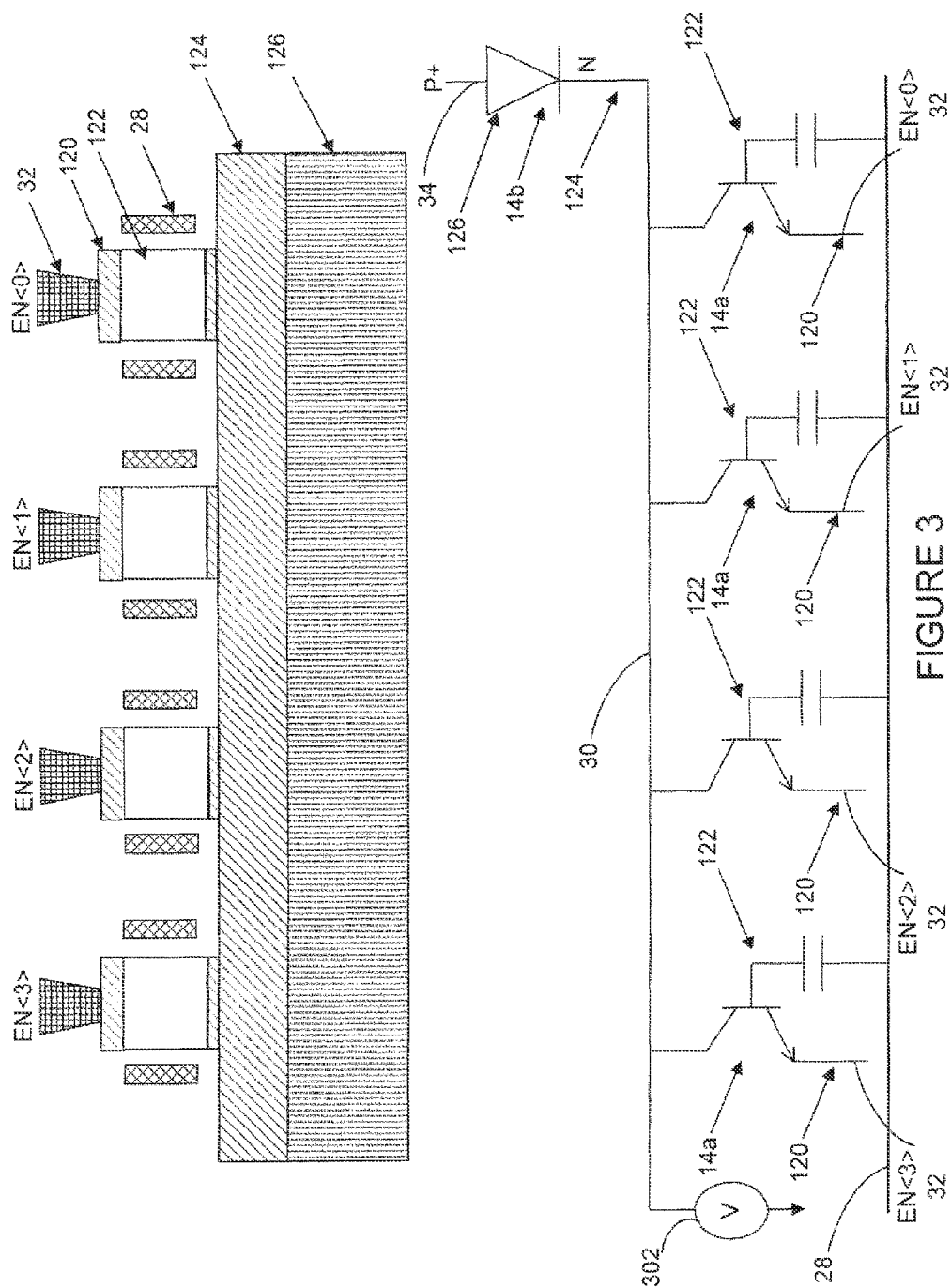


FIGURE 2



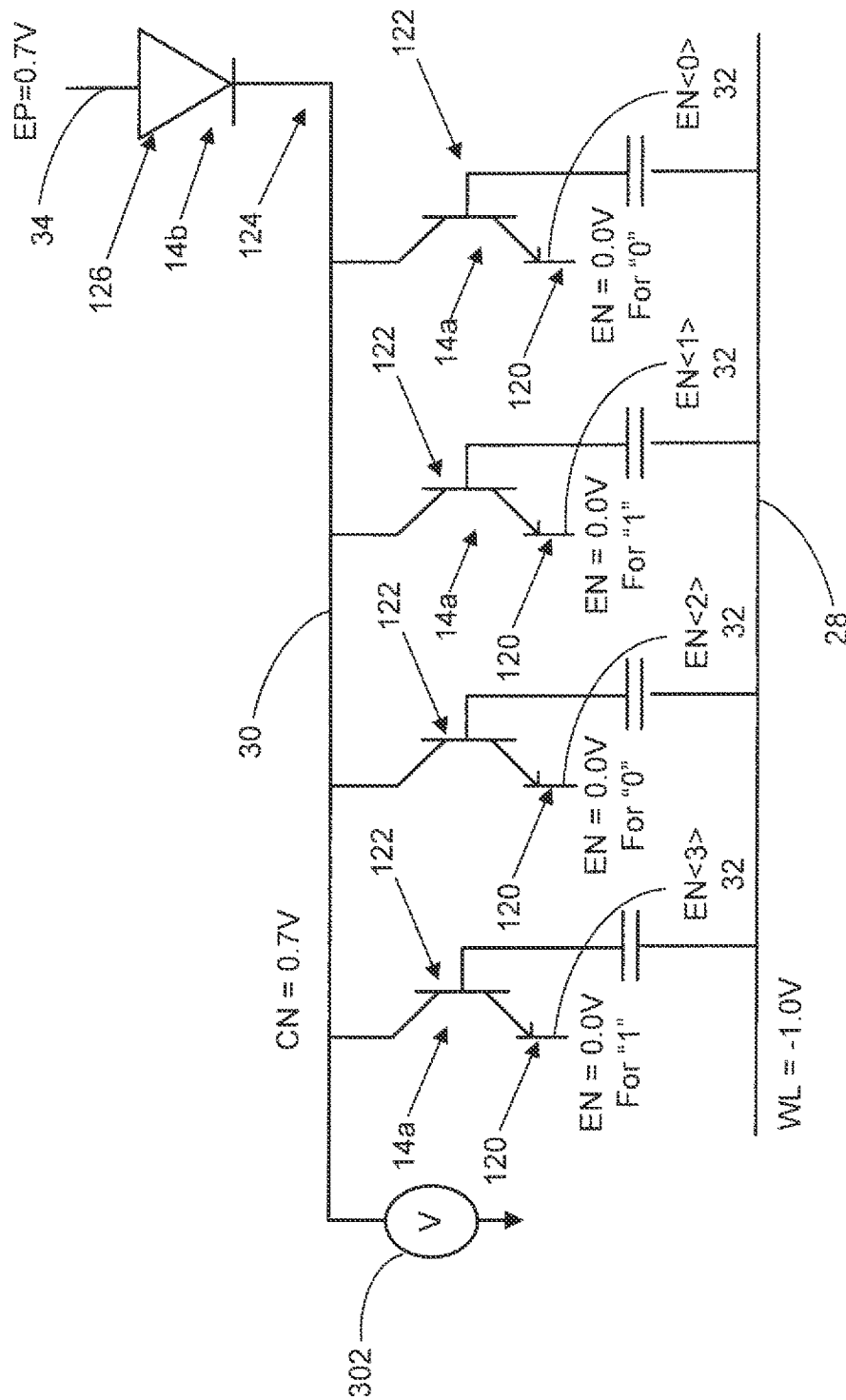


FIGURE 4A

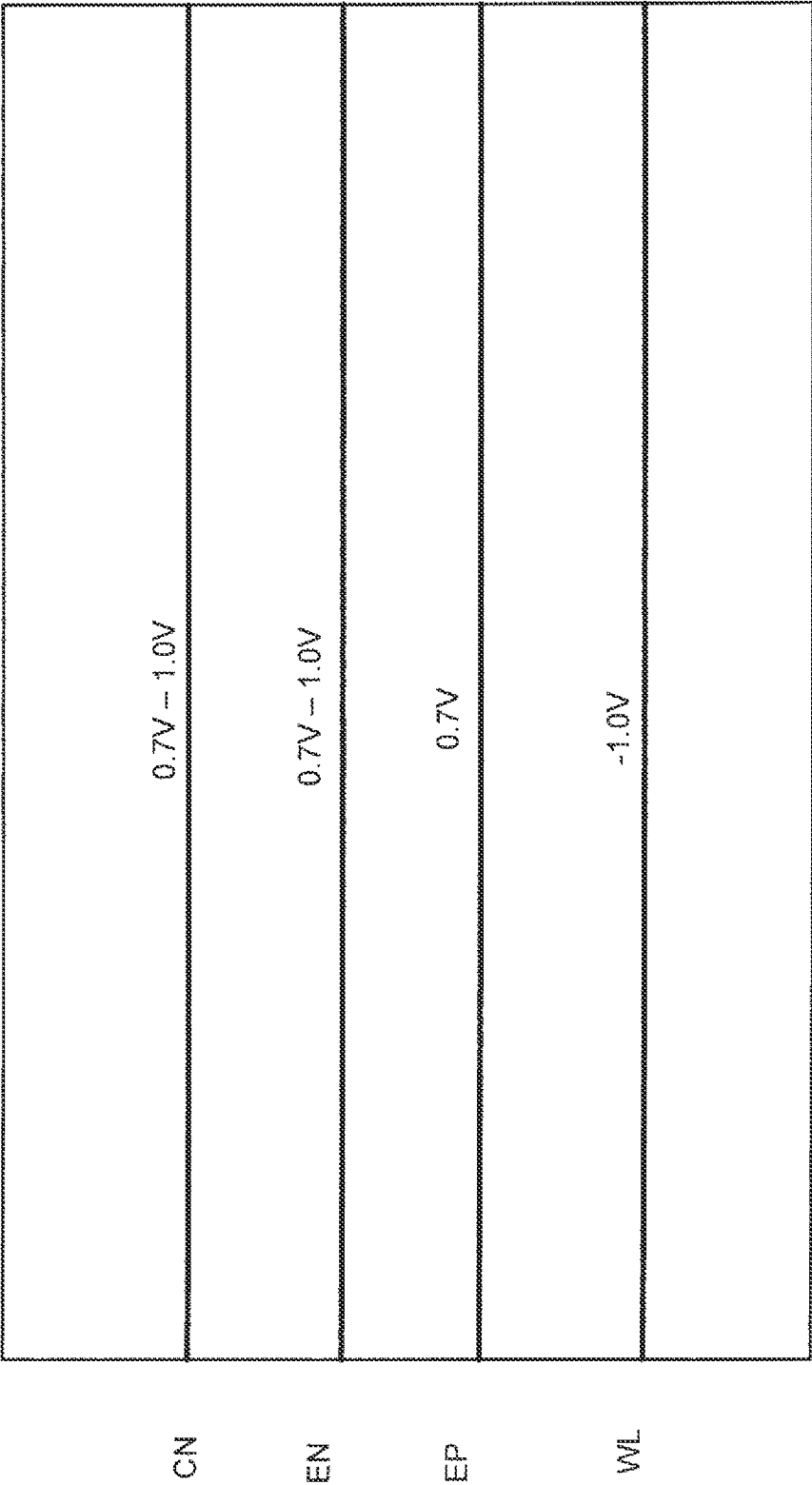


FIGURE 4B

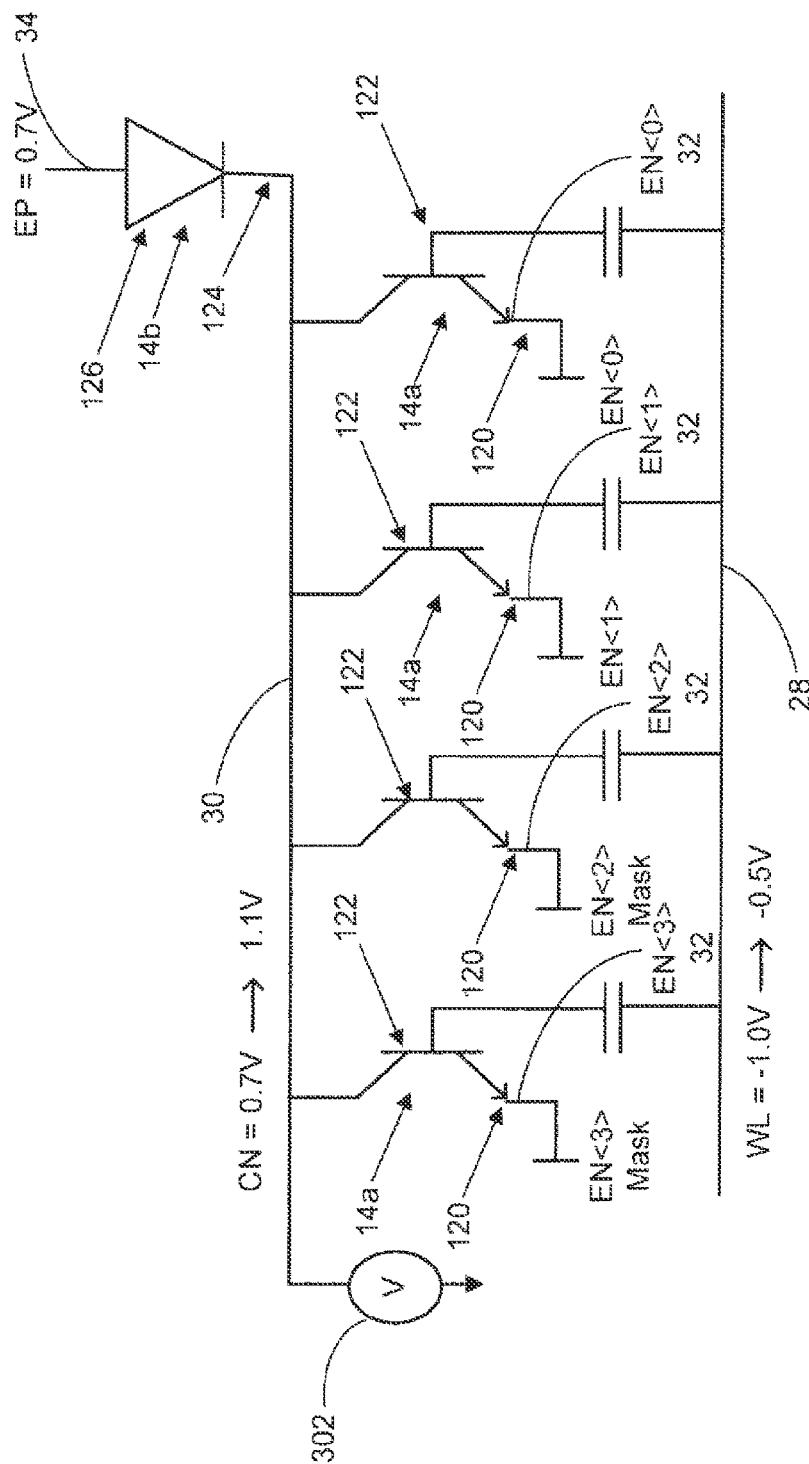


FIGURE 5A

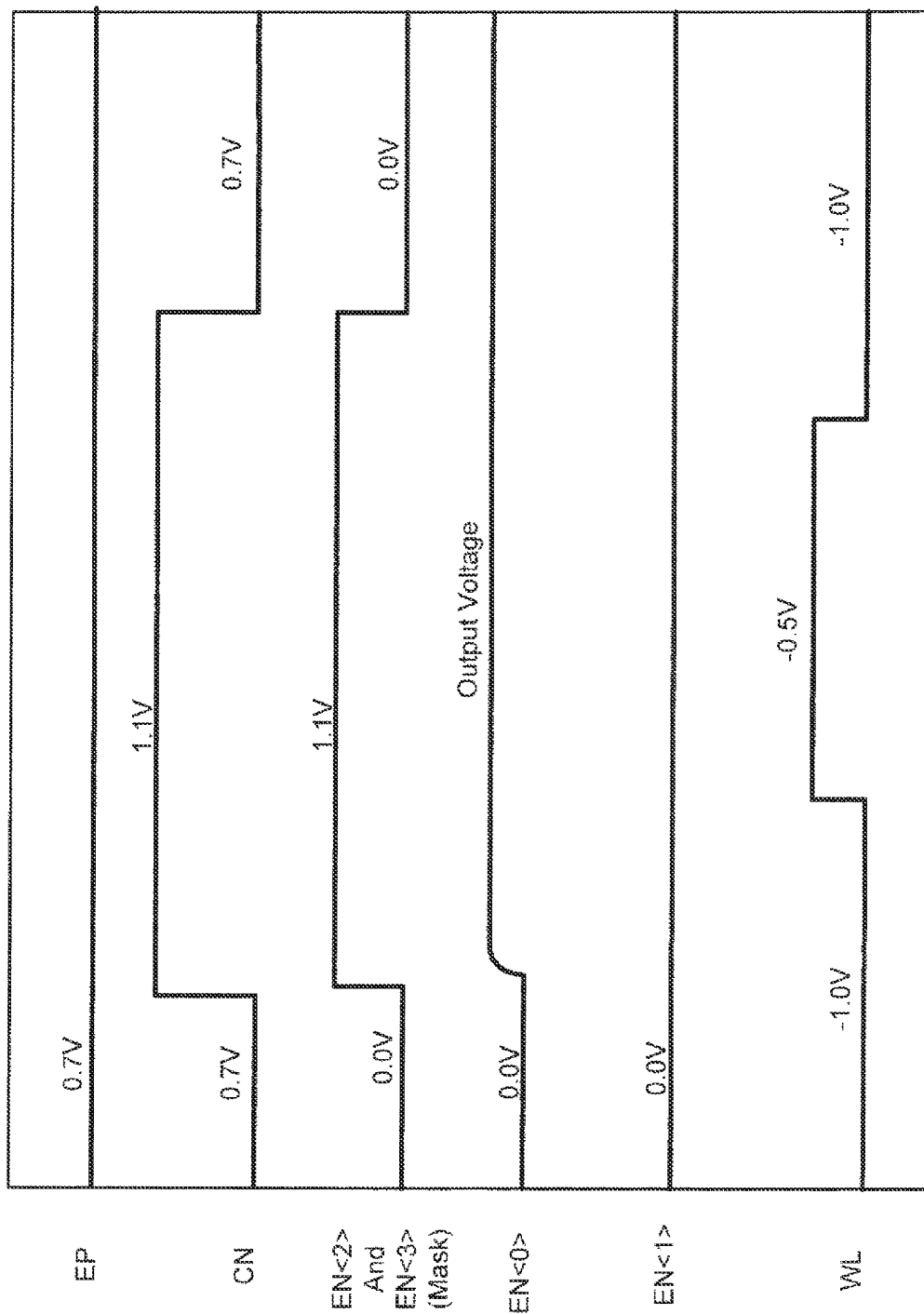


FIGURE 5B

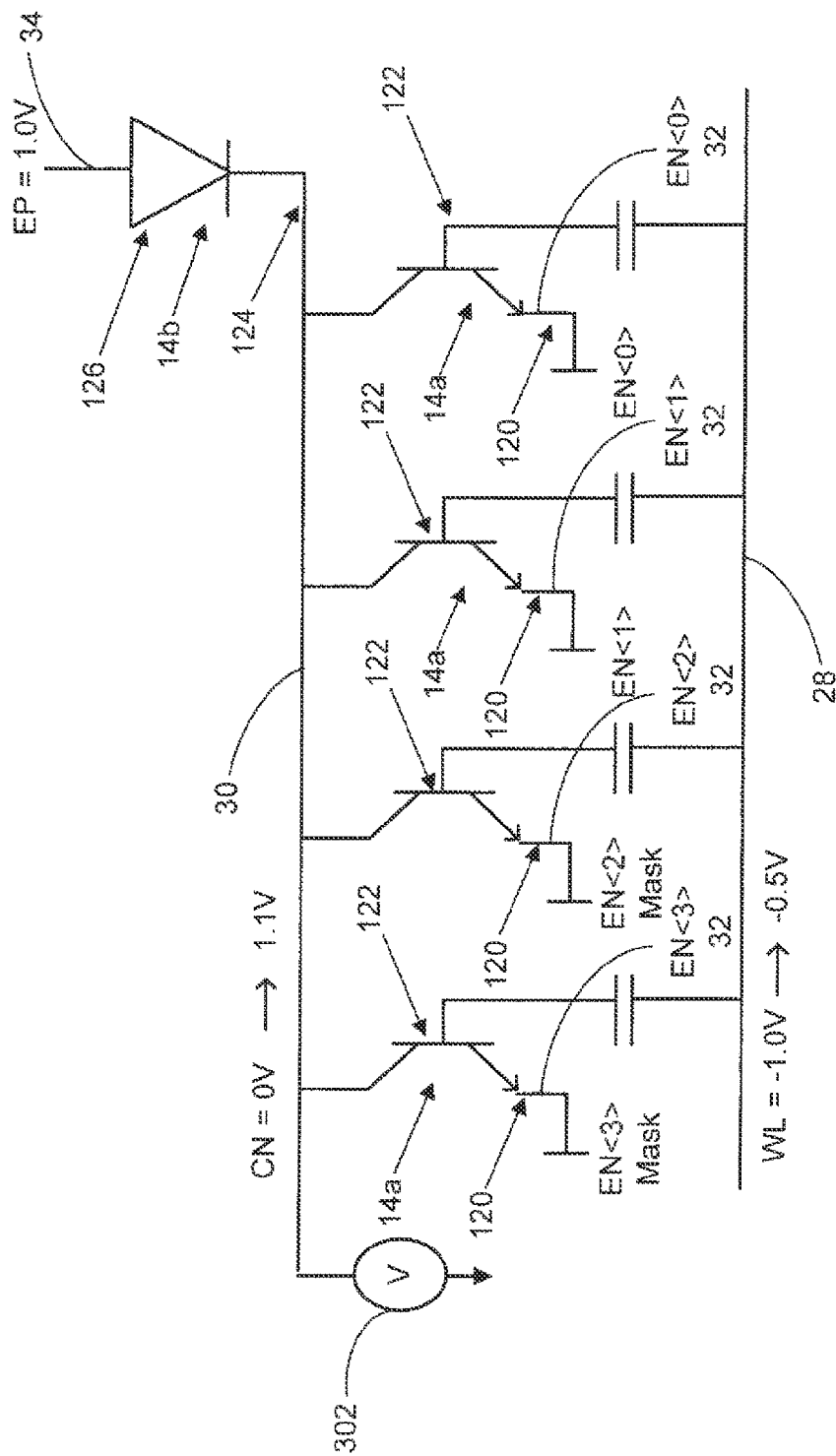


FIGURE 6A

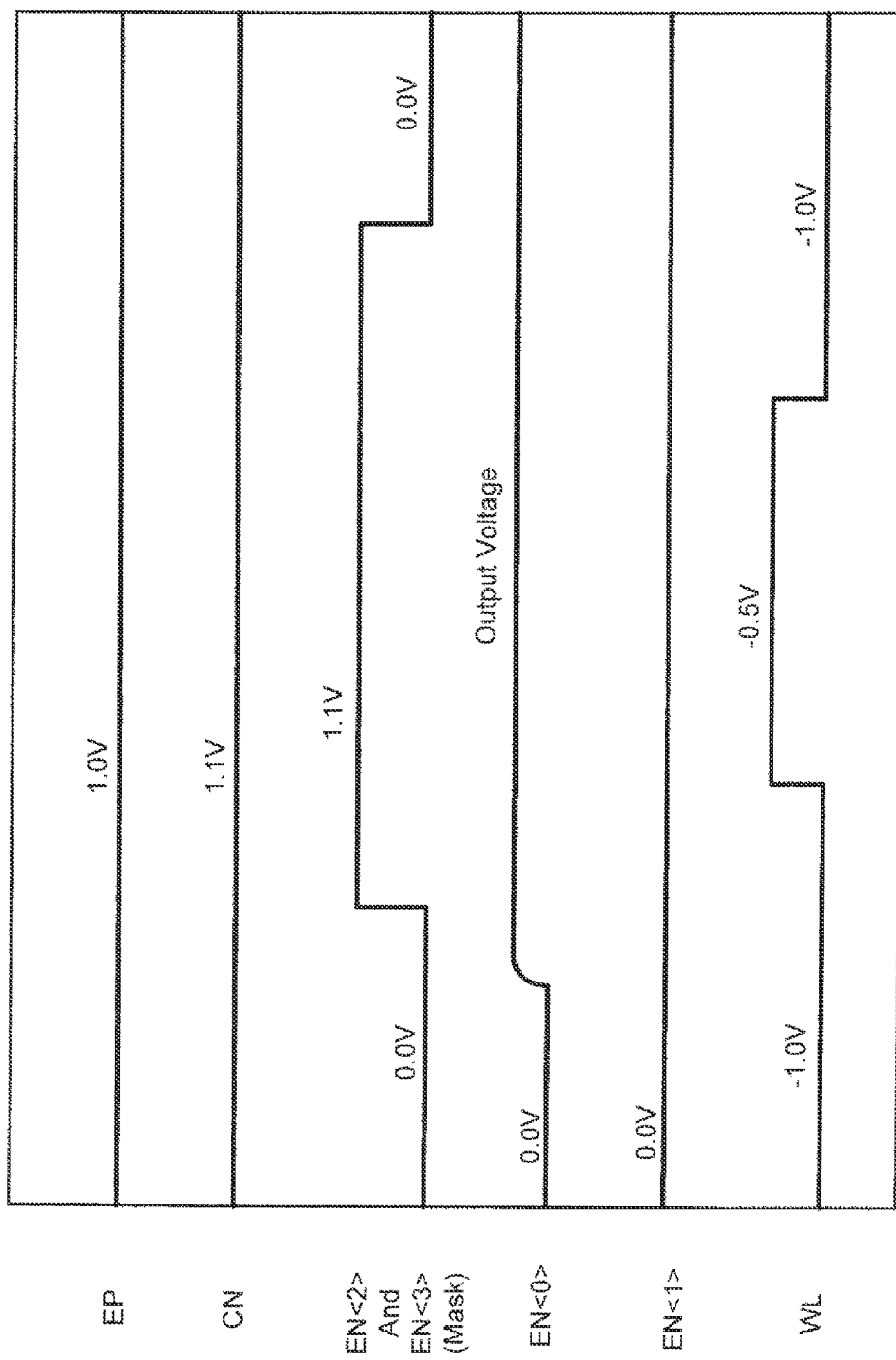


FIGURE 6B

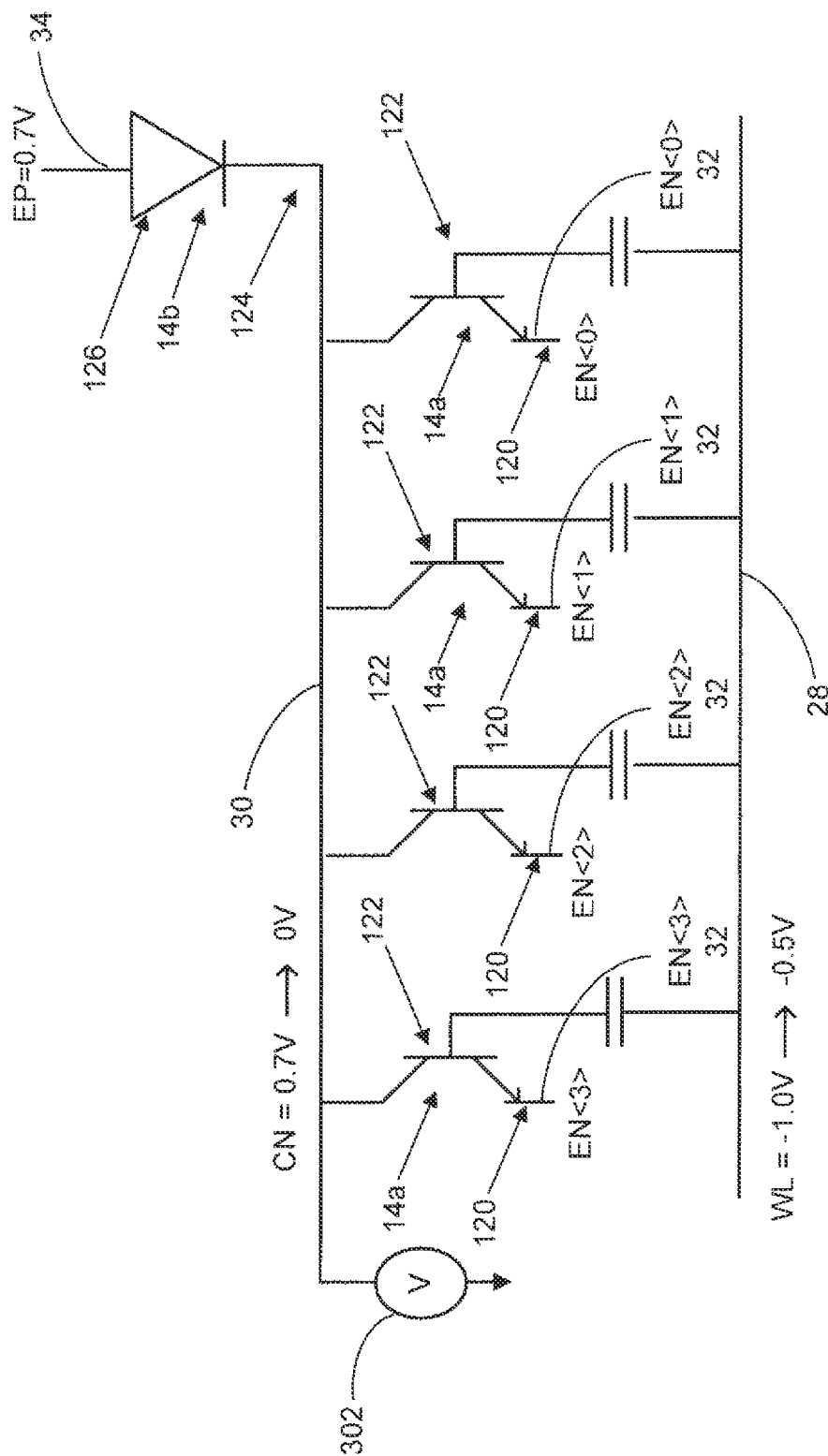


FIGURE 7A

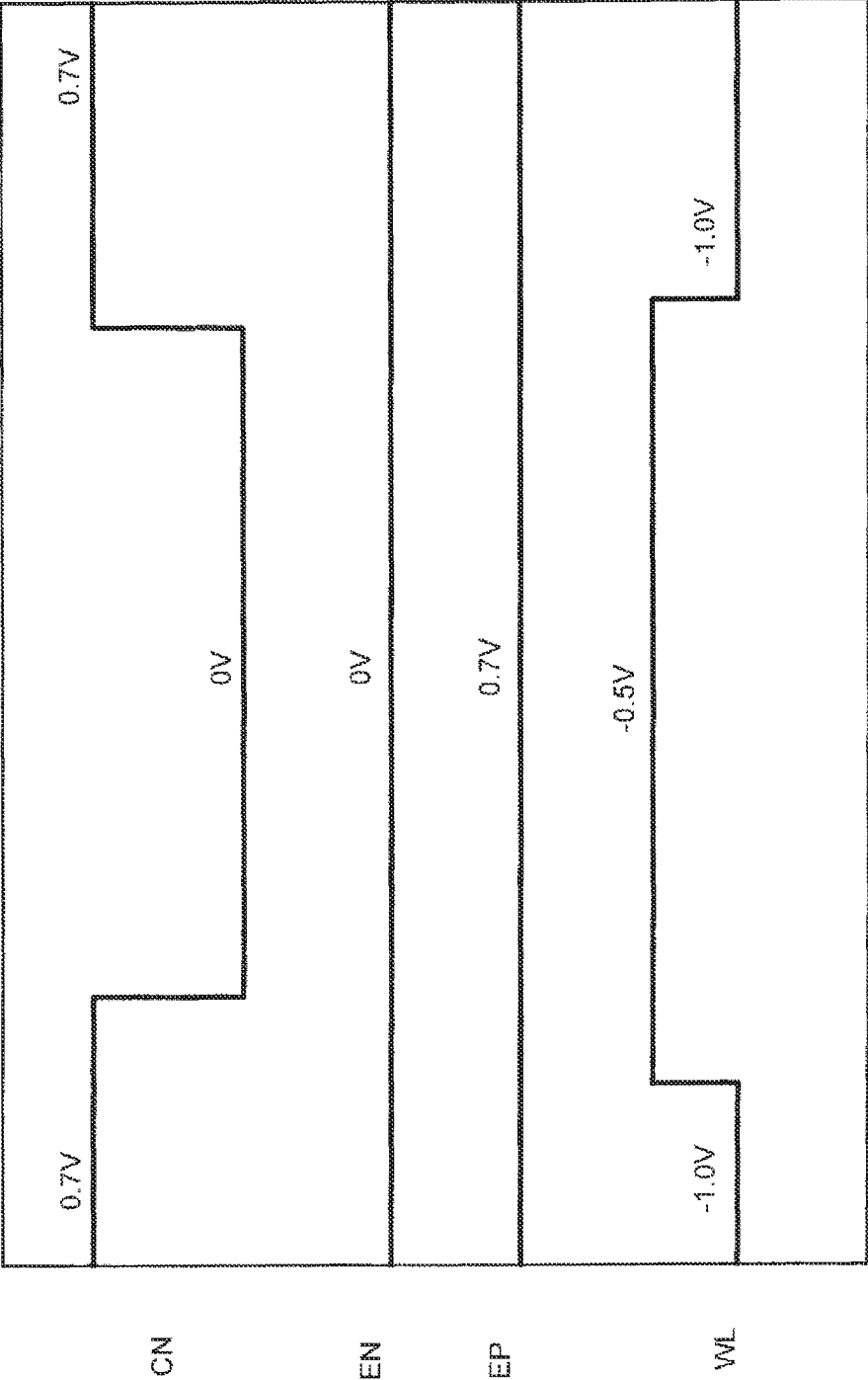


FIGURE 7B

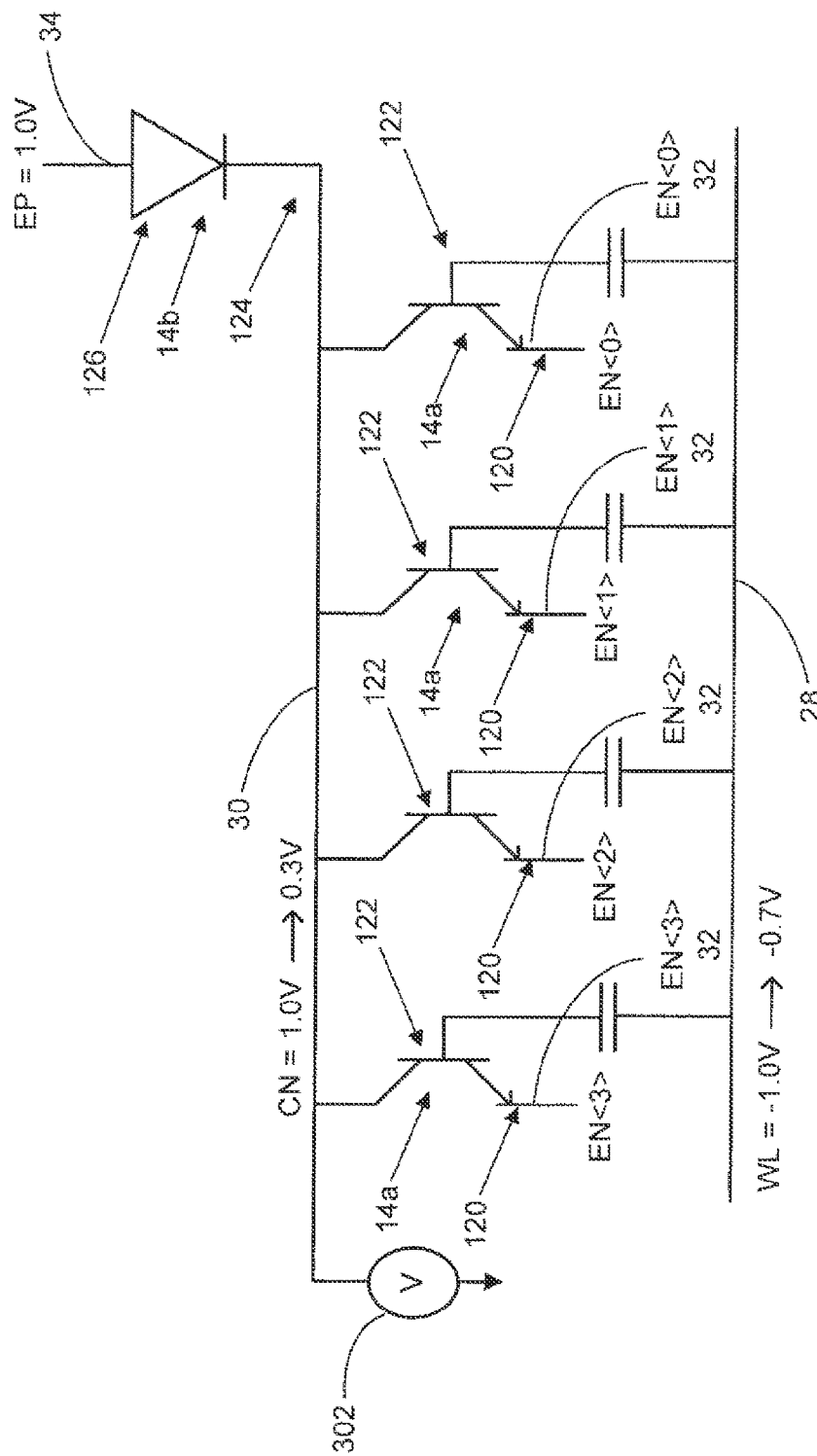


FIGURE 8A

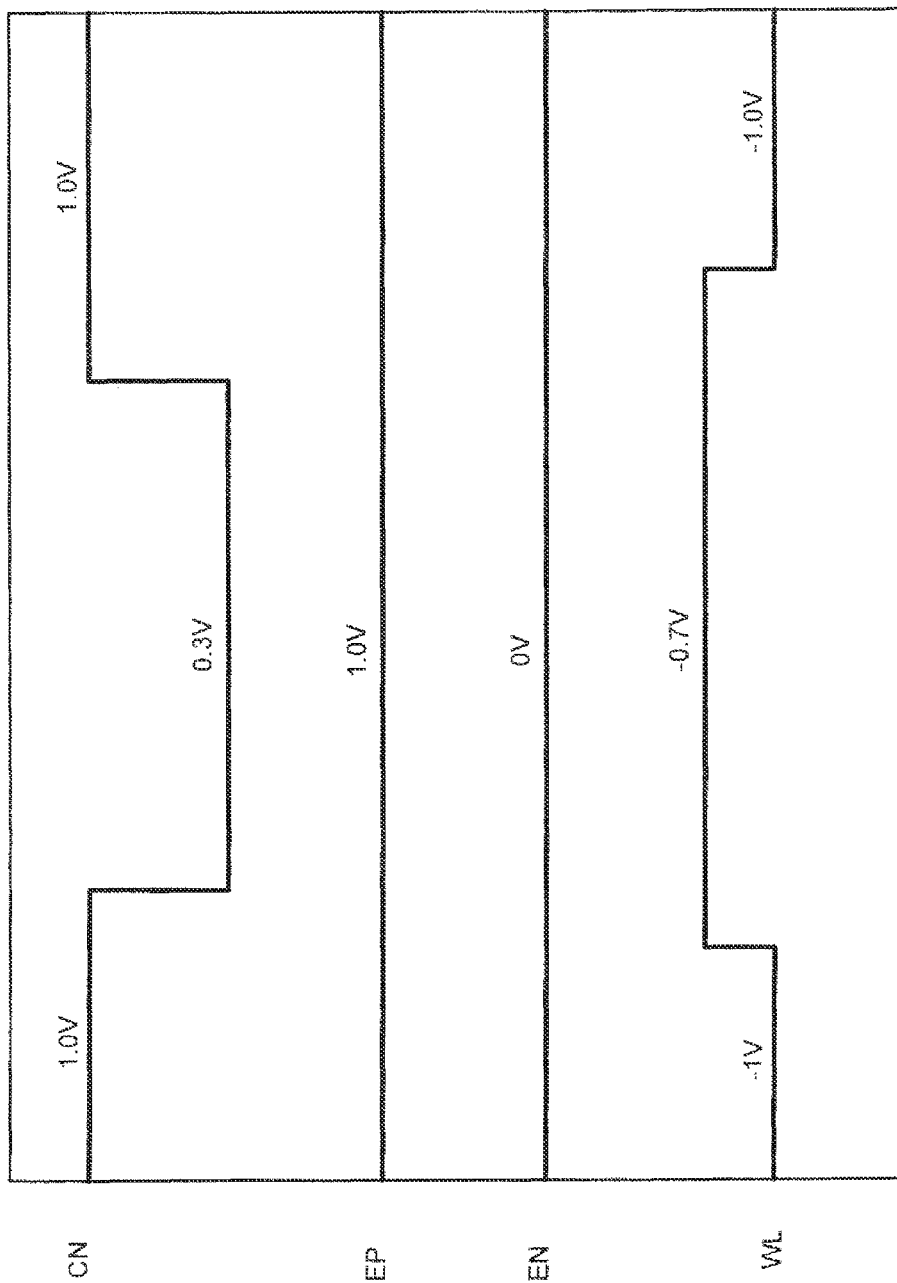


FIGURE 8B

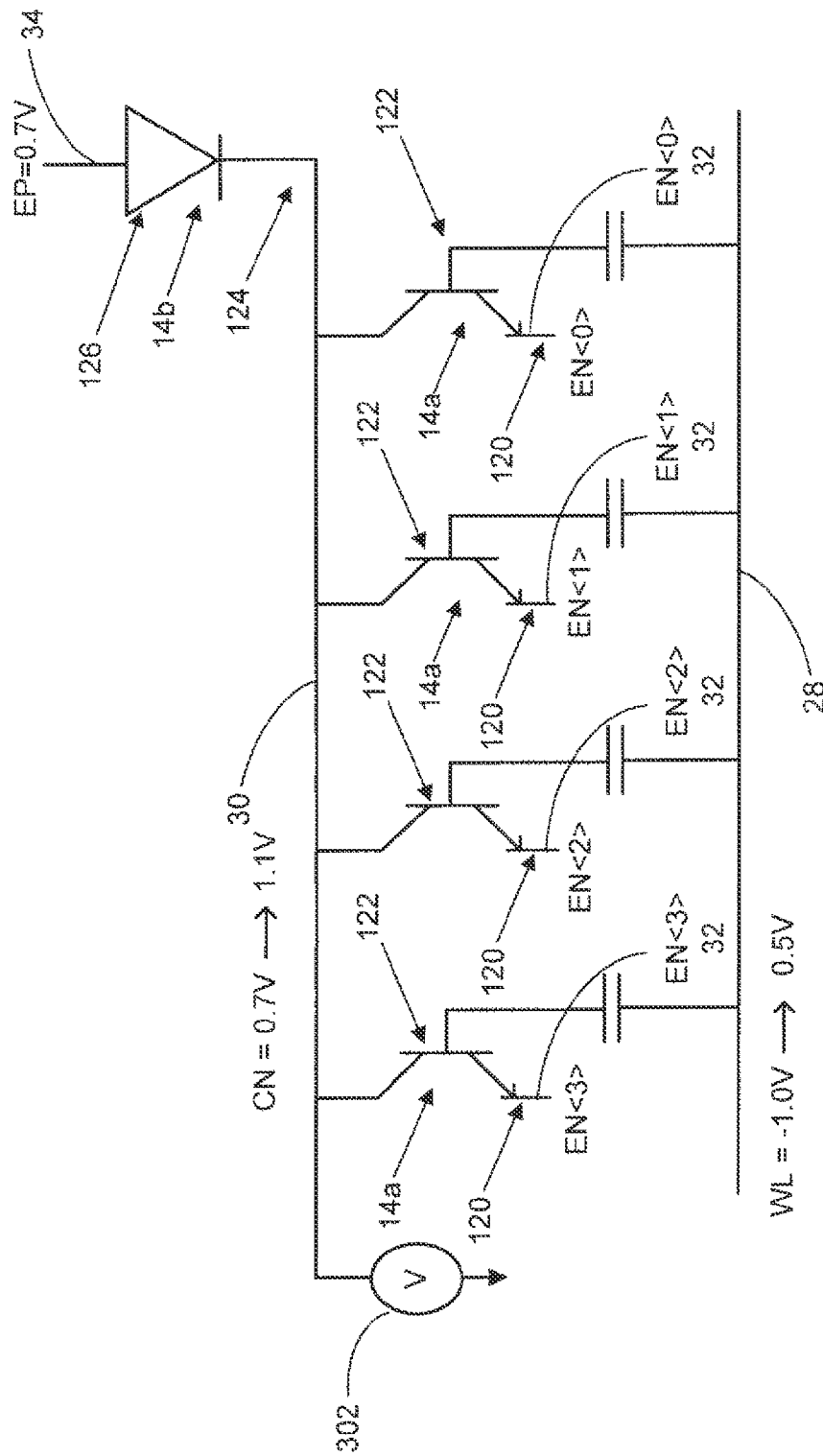


FIGURE 9A

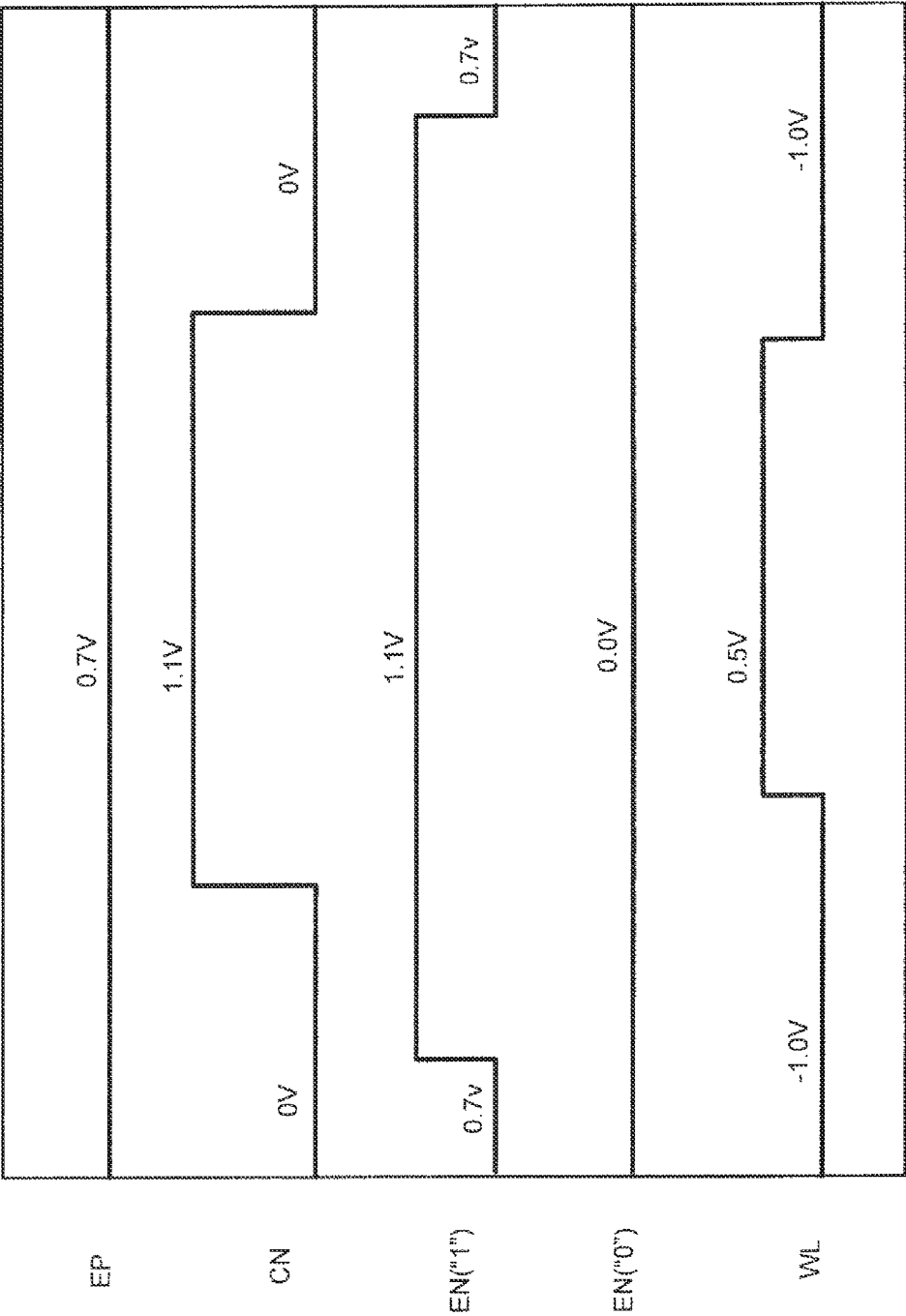


FIGURE 9B

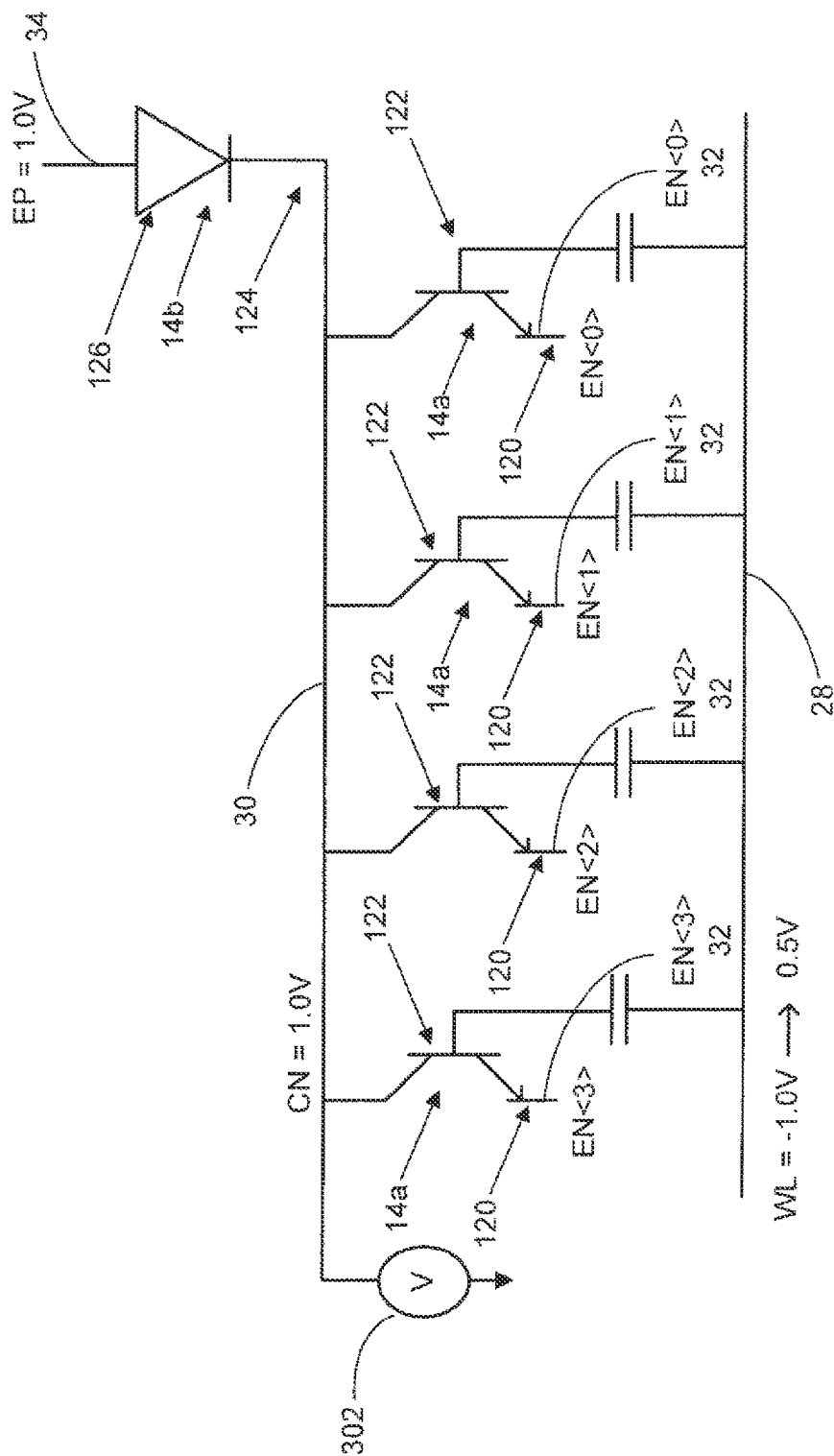


FIGURE 10A

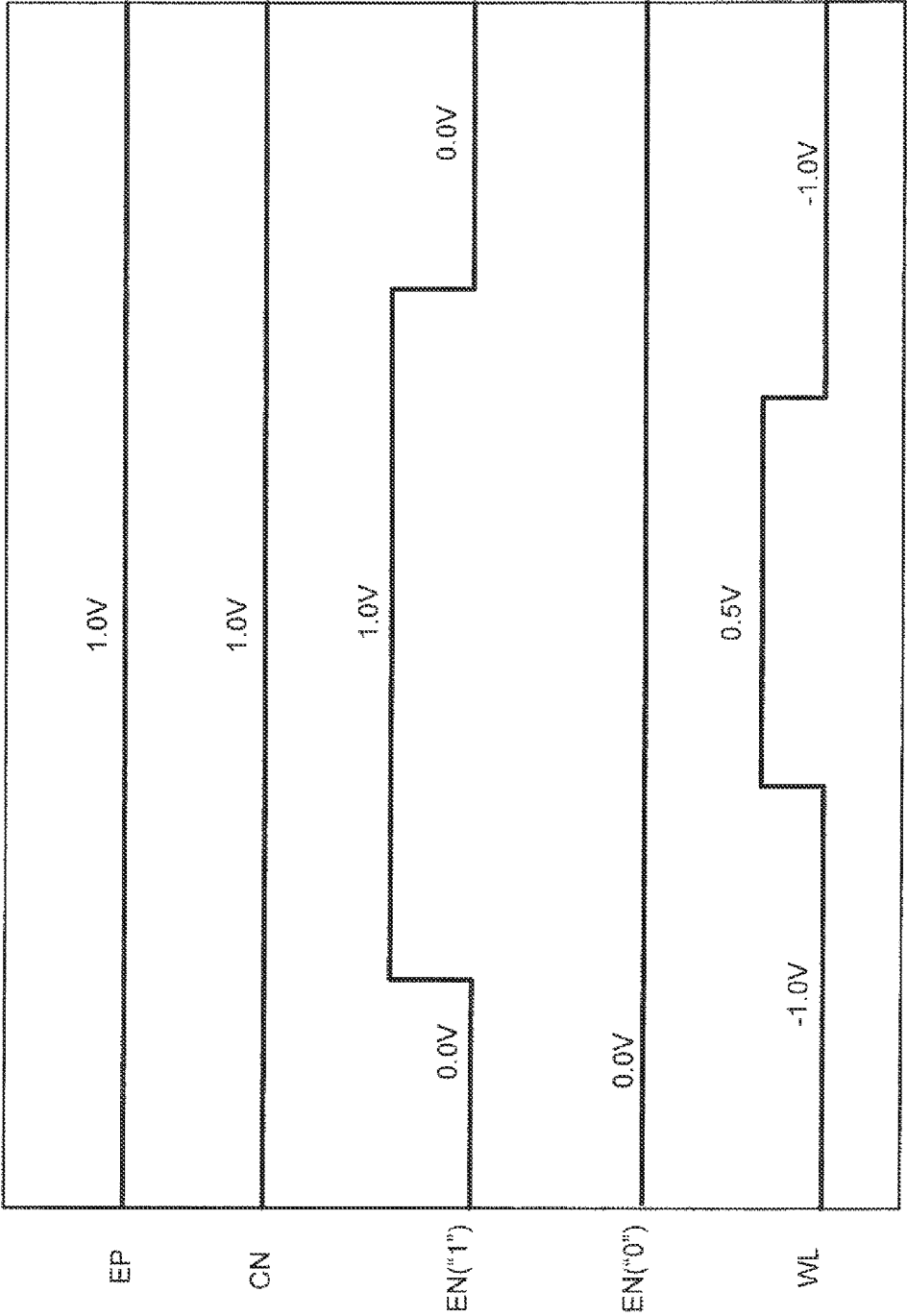


FIGURE 10B

TECHNIQUES FOR PROVIDING A DIRECT INJECTION SEMICONDUCTOR MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

This patent application is a continuation of U.S. patent application Ser. No. 13/964,927, filed Aug. 12, 2013, which is a continuation of U.S. patent application Ser. No. 12/768,322, filed Apr. 27, 2010, now U.S. Pat. No. 8,508,970, issued Aug. 13, 2013, which claims priority to U.S. Provisional Patent Application No. 61/173,014, filed Apr. 27, 2009, each of which is hereby incorporated by reference herein in its entirety.

FIELD OF THE DISCLOSURE

The present disclosure relates generally to semiconductor memory devices and, more particularly, to techniques for providing a direct injection semiconductor memory device.

BACKGROUND OF THE DISCLOSURE

The semiconductor industry has experienced technological advances that have permitted increases in density and/or complexity of semiconductor memory devices. Also, the technological advances have allowed decreases in power consumption and package sizes of various types of semiconductor memory devices. There is a continuing trend to employ and/or fabricate advanced semiconductor memory devices using techniques, materials, and devices that improve performance, reduce leakage current, and enhance overall scaling. Silicon-on-insulator (SOI) and bulk substrates are examples of materials that may be used to fabricate such semiconductor memory devices. Such semiconductor memory devices may include, for example, partially depleted (PD) devices, fully depleted (FD) devices, multiple gate devices (for example, double, triple gate, or surrounding gate), and Fin-FET devices.

A semiconductor memory device may include a memory cell having a memory transistor with an electrically floating body region wherein electrical charges may be stored. When excess majority electrical charges carriers are stored in the electrically floating body region, the memory cell may store a logic high (e.g., binary "1" data state). When the electrical floating body region is depleted of majority electrical charge carriers, the memory cell may store a logic low (e.g., binary "0" data state). Also, a semiconductor memory device may be fabricated on silicon-on-insulator (SOI) substrates or bulk substrates (e.g., enabling body isolation). For example, a semiconductor memory device may be fabricated as a three-dimensional (3-D) device (e.g., multiple gate devices, Fin-FETs, recessed gates and pillars).

In one conventional technique, the memory cell of the semiconductor memory device may be read by applying bias signals to a source/drain region and/or a gate of the memory transistor. As such, a conventional reading technique may involve sensing an amount of current provided/generated by/in the electrically floating body region of the memory cell in response to the application of the source/drain region or gate bias signals to determine a data state stored in the memory cell. For example, the memory cell may have two or more different current states corresponding to two or more different logical states (e.g., two different current conditions/ states corresponding to two different logic states: a binary "0" data state and a binary "1" data state).

In another conventional technique, the memory cell of the semiconductor memory device may be written to by applying bias signals to the source/drain region(s) and/or the gate of the memory transistor. As such, a conventional writing technique may result in an increase/decrease of majority charge carriers in the electrically floating body region of the memory cell which, in turn, may determine the data state of the memory cell. An increase of majority charge carriers in the electrically floating body region may result from impact ionization, band-to-band tunneling (gate-induced drain leakage "GIDL"), or direct injection. A decrease of majority charge carriers in the electrically floating body region may result from charge carriers being removed via drain region charge carrier removal, source region charge carrier removal, or drain and source region charge carrier removal, for example, using back gate pulsing.

Often, conventional reading and/or writing operations may lead to relatively large power consumption and large voltage potential swings which may cause disturbance to unselected memory cells in the semiconductor memory device. Also, pulsing between positive and negative gate biases during read and write operations may reduce a net quantity of majority charge carriers in the electrically floating body region of the memory cell in the semiconductor memory device, which, in turn, may result in an inaccurate determination of the state of the memory cell. Furthermore, in the event that a bias is applied to the gate of the memory transistor that is below a threshold voltage potential of the memory transistor, a channel of minority charge carriers beneath the gate may be eliminated. However, some of the minority charge carriers may remain "trapped" in interface defects. Some of the trapped minority charge carriers may recombine with majority charge carriers, which may be attracted to the gate as a result of the applied bias. As a result, the net quantity of majority charge carriers in the electrically floating body region may be reduced. This phenomenon, which is typically characterized as charge pumping, is problematic because the net quantity of majority charge carriers may be reduced in the electrically floating body region of the memory cell, which, in turn, may result in an inaccurate determination of the state of the memory cell.

In view of the foregoing, it may be understood that there may be significant problems and shortcomings associated with conventional techniques for fabricating and/or operating semiconductor memory devices.

SUMMARY OF THE DISCLOSURE

Techniques for providing a direct injection semiconductor memory device are disclosed. In one particular exemplary embodiment, the techniques may be realized as a method for biasing a direct injection semiconductor memory device. The method may comprise applying a first voltage potential to a first N-doped region via a bit line and applying a second voltage potential to a second N-doped region via a source line. The method may also comprise applying a third voltage potential to a word line, wherein the word line is spaced apart from and capacitively coupled to a body region that is electrically floating and disposed between the first N-doped region and the second N-doped region. The method may further comprise applying a fourth voltage potential to a P-type substrate via a carrier injection line.

In accordance with other aspects of this particular exemplary embodiment, the method may further comprise increasing the third voltage potential applied to the word line

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from the third voltage potential applied to the word line during a hold operation to perform a read operation.

In accordance with further aspects of this particular exemplary embodiment, the method may further comprise increasing the second voltage potential applied to the source line from the second voltage potential applied to the source line during a hold operation to perform a read operation.

In accordance with additional aspects of this particular exemplary embodiment, the method may further comprise maintaining the second voltage potential applied to the source line during a hold operation to perform a read operation.

In accordance with yet another aspect of this particular exemplary embodiment, the method may further comprise increasing the first voltage potential applied to the bit line from the first voltage potential applied to the bit line during a hold operation in order to reduce a disturbance during a read operation.

In accordance with other aspects of this particular exemplary embodiment, the method may further comprise increasing the third voltage potential applied to the word line from the third voltage potential applied to the word line during a hold operation to perform a write logic high operation.

In accordance with further aspects of this particular exemplary embodiment, the method may further comprise lowering the second voltage potential applied to the source line from the second voltage potential applied to the source line during a hold operation to perform a write logic high operation.

In accordance with additional aspects of this particular exemplary embodiment, the second voltage potential applied to the source line to perform the write logic high operation may be lowered to forward bias a junction between the second N-doped region and the P-type substrate.

In accordance with yet another aspect of this particular exemplary embodiment, the method may further comprise increasing the third voltage potential applied to the respective word line from the third voltage potential applied to the respective word line during a hold operation to perform a write logic low operation.

In accordance with other aspects of this particular exemplary embodiment, the method may further comprise increasing the second voltage potential applied to the source line from the second voltage potential applied to the source line during a hold operation to perform a write logic low operation.

In accordance with further aspects of this particular exemplary embodiment, the method may further comprise maintaining the second voltage potential applied to the source line during a hold operation to perform a write logic low operation.

In accordance with additional aspects of this particular exemplary embodiment, the method may further comprise maintaining the first voltage potential applied to the bit line during a hold operation to perform a write logic low operation.

In accordance with yet another aspect of this particular exemplary embodiment, the method may further comprise increasing the first voltage potential applied to the bit line during a write logic low operation from the first voltage potential applied to the bit line during a hold operation to maintain a logic high stored in the memory cell.

In accordance with other aspects of this particular exemplary embodiment, the second voltage potential applied to

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the source line may be equal to the fourth voltage potential applied to the carrier injection line during a hold operation.

In another particular exemplary embodiment, the techniques may be realized as a direct injection semiconductor memory device comprising a first N-doped region coupled to a bit line and a second N-doped region coupled to a source line. The direct injection semiconductor memory device may also comprise a body region spaced apart from and capacitively coupled to a word line, wherein the body region is electrically floating and disposed between the first N-doped region and the second N-doped region. The direct injection semiconductor memory device may further comprise a P-type substrate coupled to a carrier injection line.

In accordance with other aspects of this particular exemplary embodiment, the first N-doped region, the body region, and the second N-doped region may form a bipolar transistor.

In accordance with further aspects of this particular exemplary embodiment, the second N-doped region and the P-type substrate may form a PN junction diode.

In accordance with additional aspects of this particular exemplary embodiment, the bit line may extend from the first N-doped region perpendicular to at least a portion of at least one of the source line, the word line, and the carrier injection line.

In accordance with yet another aspect of this particular exemplary embodiment, the word line may extend from near the body region horizontally parallel to at least a portion of at least one of the source line and the carrier injection line.

In accordance with other aspects of this particular exemplary embodiment, the source line may extend from the second N-doped region parallel to at least one of the word line and the carrier injection line.

In another exemplary embodiment, the techniques may be realized as a method for biasing a direct injection semiconductor memory device. The method may comprise applying a first voltage potential to a first P-doped region via a bit line and applying a second voltage potential to a second P-doped region via a source line. The method may also comprise applying a third voltage potential to a word line, wherein the word line is spaced apart from and capacitively coupled to a body region that is electrically floating and disposed between the first P-doped region and the second P-doped region. The method may further comprise applying a fourth voltage potential to an N-type substrate via a carrier injection line.

In another exemplary embodiment, the techniques may be realized as a direct injection semiconductor memory device that may comprise a first P-doped region coupled to a bit line and a second P-doped region coupled to a source line. The direct injection semiconductor memory device may also comprise a body region spaced apart from and capacitively coupled to a word line, wherein the body region is electrically floating and disposed between the first N-doped region and the second N-doped region. The direct injection semiconductor memory device may further comprise a P-type substrate coupled to a carrier injection line.

The present disclosure will now be described in more detail with reference to exemplary embodiments thereof as shown in the accompanying drawings. While the present disclosure is described below with reference to exemplary embodiments, it should be understood that the present disclosure is not limited thereto. Those of ordinary skill in the art having access to the teachings herein will recognize additional implementations, modifications, and embodiments, as well as other fields of use, which are within the

scope of the present disclosure as described herein, and with respect to which the present disclosure may be of significant utility.

BRIEF DESCRIPTION OF THE DRAWINGS

In order to facilitate a fuller understanding of the present disclosure, reference is now made to the accompanying drawings, in which like elements are referenced with like numerals. These drawings should not be construed as limiting the present disclosure, but are intended to be exemplary only.

FIG. 1 shows a block diagram of a semiconductor memory device including a memory cell array, data write and sense circuitry, and memory cell selection and control circuitry in accordance with an embodiment of the present disclosure.

FIG. 2 shows a cross-sectional view and a schematic representation of a memory cell in the memory cell array shown in FIG. 1 in accordance with an embodiment of the present disclosure.

FIG. 3 shows a cross-sectional view and a schematic representation of at least a portion of the memory cell array having the plurality of memory cells in accordance with an embodiment of the present disclosure.

FIGS. 4A and 4B show a schematic representation and control signal voltage waveforms for performing a hold operation on a memory cell in accordance with an embodiment of the present disclosure.

FIGS. 5A and 5B show a schematic representation and control signal voltage waveforms for performing a read operation on a memory cell in accordance with an embodiment of the present disclosure.

FIGS. 6A and 6B show a schematic representation and control signal voltage waveforms for performing a read operation on a memory cell in accordance with an alternative embodiment of the present disclosure.

FIGS. 7A and 7B show a schematic representation and control signal voltage waveforms for performing a write logic high (e.g., binary “1” data state) operation on a memory cell in accordance with an embodiment of the present disclosure.

FIGS. 8A and 8B show a schematic representation and control signal voltage waveforms for performing a write logic high (e.g., binary “1” data state) operation on a memory cell in accordance with an alternative embodiment of the present disclosure.

FIGS. 9A and 9B show a schematic representation and control signal voltage waveforms for performing a write logic low (e.g., binary “0” data state) operation on a memory cell in accordance with an embodiment of the present disclosure.

FIGS. 10A and 10B show a schematic representation and control signal voltage waveforms for performing a write logic low (e.g., binary “0” data state) operation on a memory cell in accordance with an alternative embodiment of the present disclosure.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Referring to FIG. 1, there is shown a block diagram of a semiconductor memory device 10 comprising a memory cell array 20, data write and sense circuitry 36, and memory cell selection and control circuitry 38 in accordance with an embodiment of the present disclosure. The memory cell array 20 may comprise a plurality of memory cells 12 each

coupled to the memory cell selection and control circuitry 38 via a word line (WL) 28, a source line (CN) 30, and a carrier injection line (EP) 34, and to the data write and sense circuitry 36 via a bit line (EN) 32. It may be appreciated that the source line (CN) 30 and the bit line (EN) 32 are designations used to distinguish between two signal lines and they may be used interchangeably.

The data write and sense circuitry 36 may read data from and may write data to selected memory cells 12. In an exemplary embodiment, the data write and sense circuitry 36 may include a plurality of data sense amplifiers. Each data sense amplifier may receive at least one bit line (EN) 32 and a current or voltage reference signal. For example, each data sense amplifier may be a cross-coupled type sense amplifier to sense a data state stored in a memory cell 12.

Each data sense amplifier may employ voltage and/or current sensing circuitry and/or techniques. In an exemplary embodiment, each data sense amplifier may employ current sensing circuitry and/or techniques. For example, a current sense amplifier may compare current from a selected memory cell 12 to a reference current (e.g., the current of one or more reference cells). From that comparison, it may be determined whether the selected memory cell 12 stores a logic high (e.g., binary “1” data state) or a logic low (e.g., binary “0” data state). It may be appreciated by one having ordinary skill in the art that various types or forms of the data write and sense circuitry 36 (including one or more sense amplifiers, using voltage or current sensing techniques, to sense a data state stored in a memory cell 12) may be employed to read data stored in memory cells 12 and/or write data to memory cells 12.

The memory cell selection and control circuitry 38 may select and/or enable one or more predetermined memory cells 12 to facilitate reading data therefrom and/or writing data thereto by applying control signals on one or more word lines (WL) 28, source lines (CN) 30, and/or carrier injection lines (EP) 34. The memory cell selection and control circuitry 38 may generate such control signals from address signals, for example, row address signals. Moreover, the memory cell selection and control circuitry 38 may include a word line decoder and/or driver. For example, the memory cell selection and control circuitry 38 may include one or more different control/selection techniques (and circuitry therefor) to select and/or enable one or more predetermined memory cells 12. Notably, all such control/selection techniques, and circuitry therefor, whether now known or later developed, are intended to fall within the scope of the present disclosure.

In an exemplary embodiment, the semiconductor memory device 10 may implement a two step write operation whereby all the memory cells 12 in a row of memory cells 12 may be written to a predetermined data state by first executing a “clear” or a logic low (e.g., binary “0” data state) write operation, whereby all of the memory cells 12 in the row of memory cells 12 are written to logic low (e.g., binary “0” data state). Thereafter, selected memory cells 12 in the row of memory cells 12 may be selectively written to the predetermined data state (e.g., a logic high (binary “1” data state)). The semiconductor memory device 10 may also implement a one step write operation whereby selective memory cells 12 in a row of memory cells 12 may be selectively written to either a logic high (e.g., binary “1” data state) or a logic low (e.g., binary “0” data state) without first implementing a “clear” operation. The semiconductor memory device 10 may employ any of the exemplary writing, preparation, holding, refresh, and/or reading techniques described herein.

The memory cells **12** may comprise N-type, P-type and/or both types of transistors. Circuitry that is peripheral to the memory array **20** (for example, sense amplifiers or comparators, row and column address decoders, as well as line drivers (not illustrated herein)) may also include P-type and/or N-type transistors. Regardless of whether P-type or N-type transistors are employed in memory cells **12** in the memory cell array **20**, suitable voltage potentials (for example, positive or negative voltage potentials) for reading from and/or writing to the memory cells **12** will be described further herein.

Referring to FIG. 2, there is shown a cross-sectional view and a schematic representation of a memory cell **12** of the memory cell array **20** shown in FIG. 1 in accordance with an embodiment of the present disclosure. Each memory cell **12** may comprise a bipolar transistor **14a** and a diode **14b**. In an exemplary embodiment, the bipolar transistor **14a** may be a NPN bipolar transistor or a PNP bipolar transistor and the diode **14b** may be a PN junction diode. In an exemplary embodiment, the bipolar transistor **14a** and the diode **14b** may share one or more common regions. The NPN bipolar transistor **14a** may comprise an N+ emitter region **120**, a P-base region **122**, and an N+ collector region **124**. The diode **14b** may comprise the N+ region **124** and a P+ region **126**. The N+ region **120**, the P- region **122**, the N+ region **124**, and/or the P+ region **126** may be disposed in sequential contiguous relationship within a pillar or fin configuration that may extend vertically from and/or perpendicularly to a plane defined by the P+ region **126**. In an exemplary embodiment, the P- region **122** may be an electrically floating body region of the memory cell **12** configured to accumulate/store charges, and may be spaced apart from and capacitively coupled to the word line (WL) **28**.

As shown in FIG. 2, the N+ emitter region **120** of the bipolar transistor **14a** may be coupled to a corresponding bit line (EN) **32**. In an exemplary embodiment, the N+ emitter region **120** of the bipolar transistor **14a** may be formed of a semiconductor material (e.g., silicon) comprising donor impurities. For example, the N+ emitter region **120** may be formed of a silicon material doped with phosphorous or arsenic impurities. In an exemplary embodiment, the bit line (EN) **32** may be formed of a metal layer. In another exemplary embodiment, the bit line (EN) **32** may be formed of a polycide layer (e.g., a combination of a metal material and a silicon material). The bit line (EN) **32** may provide means for accessing one or more selected memory cells **12** on a selected row of the memory cell array **20**.

As also shown in FIG. 2, the P- base region **122** of the bipolar transistor **14a** may be capacitively coupled to a corresponding word line (WL) **28**. In an exemplary embodiment, the P- region **122** may be formed of a semiconductor material (e.g., silicon) comprising acceptor impurities. For example, the P- region **122** may be formed of a silicon material doped with boron impurities. The P- region **122** and the word line (WL) **28** may be capacitively coupled via an insulating or dielectric material. In an exemplary embodiment, the word line (WL) **28** may be formed of a polycide layer or a metal layer extending in a row direction of the memory cell array **20**.

As further shown in FIG. 2, the N+ region **124** of the memory cell **12** may be coupled to a source line (CN) **30**. In an exemplary embodiment, the N+ region **124** may be formed of a semiconductor material (e.g., silicon) comprising donor impurities. For example, the N+ region **124** may be formed of a silicon material doped with phosphorous or arsenic impurities. In an exemplary embodiment, the source line (CN) **30** may be formed of a polycide layer. In another

exemplary embodiment, the source line (CN) **30** may be formed of a metal layer. The source line (CN) **30** may reduce a disturbance in the memory cell **12**. For example, the source line (CN) **30** may be formed of a metal layer and therefore may reduce a hole disturbance in the memory cell **12**. The source line (CN) **30** may extend horizontally in a row direction of the memory cell array **20**, parallel to the word line (WL) **28** and/or the carrier injection line (EP) **34**, and may be coupled to a plurality of memory cells **12** (e.g., a row of memory cells **12**). For example, the source line (CN) **30**, the word line (WL) **28**, and/or the carrier injection line (EP) **34** may be arranged in different planes and configured to be parallel to each other. In an exemplary embodiment, the source line (CN) **30** may be arranged in a plane between a plane containing the word line (WL) **28** and a plane containing the carrier injection line (EP) **34**.

As further shown in FIG. 2, the P+ region **126** of the diode **14b** may be coupled to the carrier injection line (EP) **34**. The P+ region **126** may be formed of a semiconductor material (e.g., silicon) comprising acceptor impurities. For example, the P+ region **126** may be formed of a silicon material doped with boron impurities. In an exemplary embodiment, a plurality of P+ regions **126** may form a base of the memory cell array **20** or a single P+ region **126** may form the base of the memory cell array **20**. Also, the P+ region **126** may be made in the form of a P-well of a bulk substrate of the memory cell array **20**.

In an exemplary embodiment, the P+ region **126** may be configured as an input region for charges to be stored in the P- region **122** of the memory cell **12**. The charges to be stored in the P- region **122** of the memory cell **12** may be supplied by the carrier injection line (EP) **34** and input into the P- region **122** via the P+ region **126** and the N+ region **124**.

The carrier injection line (EP) **34** may be formed of a polycide layer or a metal layer extending in a row direction of the memory cell array **20**. For example, the carrier injection line (EP) **34** may extend horizontally in parallel to the word line (WL) **28** and/or the source line (CN) **30**, and may be coupled to a plurality of memory cells **12** (e.g., a row of memory cells **12**). For example, the carrier injection line (EP) **34** and the word line (WL) **28** and/or the source line (CN) **30** may be arranged in different planes and configured to be parallel to each other. In an exemplary embodiment, the carrier injection line (EP) **34** may be arranged in a plane below a plane containing the word line (WL) **28** and a plane containing the source line (CN) **30**.

Referring to FIG. 3, there is shown a cross-sectional view and a schematic representation of at least a portion of the memory cell array **20** having a plurality of memory cells **12** in accordance with an embodiment of the present disclosure. As discussed above, each of the memory cells **12** may comprise a bipolar transistor **14a** and a PN junction diode **14b** coupled to each other. For example, the bipolar transistor **14a** may be an NPN bipolar transistor or a PNP bipolar transistor. As illustrated in FIG. 3, the bipolar transistor **14a** may be an NPN bipolar transistor and may share a common region (e.g., N-region) with the PN junction diode **14b**. In another exemplary embodiment, the memory transistor **14a** may be a PNP bipolar transistor and may share a common region (e.g., P-region) with the PN junction diode **14b**.

Each memory cell **12** may be coupled to a respective word line (WL) **28**, a respective source line (CN) **30**, a respective bit line (EN) **32**, and a respective carrier injection line (EP) **34**. Data may be written to or read from a selected memory cell **12** by applying suitable control signals to a selected

word line (WL) 28, a selected source line (CN) 30, a selected bit line (EN) 32, and/or a selected carrier injection line (EP) 34. In an exemplary embodiment, each word line (WL) 28, source line (CN) 30, and carrier injection line (EP) 34 may extend horizontally parallel to each other in a row direction. Each bit line (EN) 32 may extend vertically in a column direction perpendicular to each word line (WL) 28, source line (CN) 30, and/or carrier injection line (EP) 34.

In an exemplary embodiment, one or more respective bit lines (EN) 32 may be coupled to one or more data sense amplifiers (not shown) of the data write and sense circuitry 36 to read data states of one or more memory cells 12 in the column direction. A data state may be read from one or more selected memory cells 12 by applying one or more control signals to the one or more selected memory cells 12 via a selected word line (WL) 28, a selected source line (CN) 30, and/or a selected carrier injection line (EP) 34 in order to generate a voltage potential and/or a current in the one or more selected memory cells 12. The generated voltage potential and/or current may be output to the data write and sense circuitry 36 via a corresponding bit line (EN) 32 in order to read a data state stored in each selected memory cell 12.

In the event that a data state is read from a selected memory cell 12 via a selected bit line (EN) 32, then only the bit line (EN) 32 may be coupled to the data sense amplifier of the data write and sense circuitry 36. In an exemplary embodiment, the data write and sense circuitry 36 may be configured on opposite sides of the memory cell array 20.

Also, a data state may be written to one or more selected memory cells 12 by applying one or more control signals to the one or more selected memory cells 12 via a selected word line (WL) 28, a selected source line (CN) 30, a selected bit line (EN) 32, and/or a selected carrier injection line (EP) 34. The one or more control signals applied to the one or more selected memory cells 12 via a selected word line (WL) 28, a selected source line (CN) 30, a selected bit line (EN) 32, and/or a selected carrier injection line (EP) 34 may control the bipolar transistor 14a and/or the diode 14b of each selected memory cell 12 in order to write a desired data state to each selected memory cell 12.

The source line (CN) 30 may be subcircuits 302 of the memory cell selection and control circuitry 38 (e.g., driver, inverter, and/or logic circuits). The carrier injection lines (EP) 34 may be driven by subcircuits of the memory cell selection and control circuitry 38 (e.g., driver, inverter, and/or logic circuits). The subcircuits coupled to each carrier injection line (EP) 34 may be independent voltage drivers located within and/or integrated with the memory cell selection and control circuitry 38. To reduce an amount of area required by the subcircuits of the memory cell selection and control circuitry 38, a plurality of carrier injection lines (EP) 34 of the memory cell array 20 may be coupled to a single subcircuit within the memory cell selection and control circuitry 38. In an exemplary embodiment, the subcircuits of the memory cell selection and control circuitry 38 may bias a plurality of carrier injection lines (EP) 34 coupled together to different voltage potentials and/or current levels (e.g., 0V, 1.0V, etc.).

In an exemplary embodiment, during active operations (e.g., read operation or write operation), the memory cell 12 (e.g., corresponding to bit line EN<0>32) located near the subcircuits (e.g., drivers) within the memory cell selection and control circuitry 38 may be activated before the memory cells 12 (e.g., correspond to bit lines EN<1>, EN<2>, and EN<3>) located farther from the subcircuits (e.g., drivers) within the memory cell selection and control circuitry 38.

The memory cell 12 (e.g., corresponding to bit line EN<0>32) located near the subcircuits (e.g., drivers) within the memory cell selection and control circuitry 38 may impact a voltage potential and/or current applied to the source line (CN) 30. For example, when control signals are applied to the memory cell 12 (e.g., corresponding to bit line EN<0>32) located near the subcircuits (e.g., drivers) within the memory cell selection and control circuitry 38, thereby turning the bipolar transistor 14a of the memory cell 12 to an "ON" state, the actions performed by the bipolar transistor 14a of the memory cell 12 may impact a voltage potential and/or current applied to the source line (CN) 30 (e.g., raise or lower the voltage potential). Thus, the memory cell 12 (e.g., corresponding to bit line EN<0>32) located near the subcircuits (e.g., drivers) within the memory cell selection and control circuitry 38 may impact an operation performed by the memory cells 12 located farther from the subcircuits (e.g., drivers) within the memory cell selection and control circuitry 38.

Referring to FIGS. 4A and 4B, there are shown a schematic representation and control signal voltage waveforms for performing a hold operation on a memory cell in accordance with an embodiment of the present disclosure. Prior to performing one or more active operations, control signals may be configured to perform a hold operation in order to maintain a data state (e.g., a logic high (binary "1" data state) or a logic low (binary "0" data state)) stored in the memory cell 12. In particular, the control signals may be configured to perform a hold operation in order to maximize a retention time of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in the memory cell 12. Also, the control signals for the hold operation may be configured to eliminate or reduce activities or fields (e.g., electrical fields between junctions which may lead to leakage of charges) within the memory cell 12.

In an exemplary embodiment, during a hold operation, a negative voltage potential may be applied to the word line (WL) 28 that may be capacitively coupled to the P- region 122 of the memory cell 12, while a voltage potential applied to the N+ region 120 may be maintained at approximately 0V. The voltage potential applied to the N+ region 124 may be the same as the voltage potential applied to the P+ region 126. For example, the negative voltage potential applied to the word line (WL) 28 (e.g., capacitively coupled to the P- region 122 of the memory cell 12) may be -1.0V, the voltage potentials applied to the N+ region 124 and the P+ region 126 may range between 0.7V to 1.0V. During the hold operation, the junction between the N+ region 124 and the P- region 122 and the junction between the N+ region 120 and the P- region 122 may be reverse biased in order to retain a data state (e.g., a logic high (binary "1" data state) or a logic low (binary "0" data state)) stored in the memory cell 12.

Referring to FIGS. 5A and 5B, there are shown a schematic representation and control signal voltage waveforms for performing a read operation on a memory cell in accordance with an embodiment of the present disclosure. In an exemplary embodiment, a read operation may involve control signals that are configured to read a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. The control signals may be configured to predetermined voltage potentials to implement a read operation via the bit line (EN) 32. In an exemplary embodiment, a voltage potential applied to the word line (WL) 28 (e.g., capacitively coupled to the P- region 122) and/or a voltage potential

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applied to the N+ region 124 via the source line (CN) 30 may be raised to predetermined voltage potentials in order to read a data state stored in each respective memory cell 12. For example, the voltage potential applied to the word line (WL) 28 (e.g., capacitively coupled to the P- region 122 of the memory cell 12) may be raised to -0.5V from -1.0V, while the voltage potential applied to the N+ region 124 of the memory cell 12 via the source line (CN) 30 may be raised to 1.1V from 0.7V. The voltage potential applied to the carrier injection line (EP) 34 may be maintained at 0.7V.

In an exemplary embodiment, during the read operation, the voltage potential applied to the word line (WL) 28 (e.g., capacitively coupled to the P- region 122 of the memory cell 12) may be raised to -0.5V and the voltage potential applied to the source line (CN) 30 may be raised to 1.1V. Under such biasing, the junction between the P- region 122 and the N+ region 120 may become forward biased. Also, under such biasing, the junction between the P- region 122 and the N+ region 124 may be reverse biased or become weakly forward biased (e.g., above a reverse bias voltage and below a forward bias threshold voltage, or a voltage potential at a p-diffusion region in the P- region 122 may be higher than a voltage potential at an n-diffusion region in the N+ region 124). A voltage potential or current may be generated when forward biasing the junction between the P- region 122 and the N+ region 120. The voltage potential or current generated may be output to a data sense amplifier via the bit line (EN) 32 coupled to the N+ region 120. An amount of voltage potential or current generated may be representative of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in the memory cell 12.

In an exemplary embodiment, when a logic low (e.g., binary "0" data state) is stored in the memory cell 12 (e.g., corresponding to bit line (EN<1>) 32), the junction between the P- region 122 and the N+ region 120 may remain reverse biased or become weakly forward biased (e.g., above a reverse bias voltage and below a forward bias threshold voltage, or a voltage potential at a p-diffusion region in the P- region 122 may be higher than a voltage potential at an n-diffusion region in the N+ region 124). A small amount of voltage potential or current or no voltage potential or current (e.g., compared to a reference voltage potential or current) may be generated when the junction between the P- region 122 and the N+ region 120 is reverse biased or weakly forward biased. A data sense amplifier in the data write and sense circuitry 36 may detect the small amount of voltage potential or current or no voltage potential or current via the bit line (EN<1>) 32 coupled to the N+ region 120.

In another exemplary embodiment, when a logic high (e.g., binary "1" data state) is stored in the memory cell 12 (e.g., corresponding to the bit line (EN<0>) 32), the junction between the P- region 122 and the N+ region 120 may be forward biased. A larger amount of voltage potential or current (e.g., compared to a reference voltage potential or current) may be generated when the junction between the P- region 122 and the N+ region 120 is forward biased. A data sense amplifier in the data write and sense circuitry 36 may detect the larger amount of voltage potential or current via the bit line (EN<0>) 32 coupled to the N+ region 120.

During one or more active operations (e.g., read operation, write operation, sense operation, preparation to start/end operation, and/or refresh operation), voltage potentials may be applied to every memory cell 12 along an active row via a corresponding word line (WL) 28, a corresponding source line (CN) 30, and/or a corresponding carrier injection line (EP) 34. However, while the active operations may be

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performed on one or more selected memory cells 12 along the active row, one or more unselected memory cells 12 (e.g., corresponding to bit lines (EN<2>) and (EN<3>) 32) along the active row may experience a disturbance caused by the voltage potentials applied via the corresponding word line (WL) 28, the corresponding source line (CN) 30, and/or the corresponding carrier injection line (EP) 34 during the active operations. In order to reduce a disturbance experienced by the one or more unselected memory cells 12 (e.g., corresponding to bit lines (EN<2>) and (EN<3>) 32) along the active row, a masking operation may be performed on the one or more unselected memory cells 12.

In an exemplary embodiment, during a masking operation, a voltage potential may be applied to the one or more unselected memory cells 12 on an active row via corresponding bit lines (EN<2>) and (EN<3>) 32. The voltage potential applied via the corresponding bit lines (EN<2>) and (EN<3>) 32 to the one or more unselected memory cells 12 on the active row may be raised to a predetermined voltage potential. In an exemplary embodiment, the voltage potential applied to the corresponding bit lines (EN<2>) and (EN<3>) 32 associated with the one or more unselected memory cells 12 along the active row may be 1.1V in order to reduce a disturbance caused by the other voltage potentials applied during the active operations.

Referring to FIGS. 6A and 6B, there are shown a schematic representation and control signal voltage waveforms for performing a read operation on a memory cell in accordance with an alternative embodiment of the present disclosure. In an exemplary embodiment, a read operation may involve control signals that are configured to read a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. The control signals may be configured to predetermined voltage potentials to implement a read operation via the bit line (EN) 32. In an exemplary embodiment, a voltage potential applied to the word line (WL) 28 (e.g., capacitively coupled to the P- region 122) may be raised to a predetermined voltage potential. A voltage potential applied to the N+ region 124 via the source line (CN) 30 may be maintained at a predetermined voltage potential in order to read a data state stored in the memory cell 12. For example, the voltage potential applied to the word line (WL) 28 (e.g., capacitively coupled to the P- region 122 of the memory cell 12) may be raised to -0.5V from -1.0V, while the voltage potential applied to the N+ region 124 of the memory cell 12 via the source line (CN) 30 may be maintained at 1.1V. The voltage potential applied to the carrier injection line (EP) 34 may be maintained at 1.0V.

Under such biasing, the junction between the P- region 122 and the N+ region 120 may become forward biased. Also, under such biasing, the junction between the P- region 122 and the N+ region 124 may be reverse biased or become weakly forward biased (e.g., above a reverse bias voltage and below a forward bias threshold voltage, or a voltage potential at a p-diffusion region in the P- region 122 may be higher than a voltage potential at an n-diffusion region in the N+ region 124). A voltage potential or current may be generated when forward biasing the junction between the P- region 122 and the N+ region 120. The voltage potential or current generated may be output to a data sense amplifier via the bit line (EN) 32 coupled to the N+ region 120. An amount of voltage potential or current generated may be representative of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in the memory cell 12.

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In an exemplary embodiment, when a logic low (e.g., binary “0” data state) is stored in the memory cell 12 (e.g., corresponding to the bit line (EN<1>) 32), the junction between the P- region 122 and the N+ region 120 may remain reverse biased or become weakly forward biased (e.g., above a reverse bias voltage and below a forward bias threshold voltage, or a voltage potential at a p-diffusion region in the P- region 122 may be higher than a voltage potential at an n-diffusion region in the N+ region 124). A small amount of voltage potential or current or no voltage potential or current (e.g., compared to a reference voltage potential or current) may be generated when the junction between the P- region 122 and the N+ region 120 is reverse biased or weakly forward biased. A data sense amplifier in the data write and sense circuitry 36 may detect the small amount of voltage potential or current or no voltage potential or current via the bit line (EN<1>) 32 coupled to the N+ region 120.

In another exemplary embodiment, when a logic high (e.g., binary “1” data state) is stored in the memory cell 12 (e.g., corresponding to the bit line (EN<0>) 32), the junction between the P- region 122 and the N+ region 120 may be forward biased. A larger amount of voltage potential or current (e.g., compared to a reference voltage potential or current) may be generated when the junction between the P- region 122 and the N+ region 120 is forward biased. A data sense amplifier in the data write and sense circuitry 36 may detect the larger amount of voltage potential or current via the bit line (EN<0>) 32 coupled to the N+ region 120.

During one or more active operations (e.g., read operation, write operation, sense operation, preparation to start/end operation, and/or refresh operation), voltage potentials may be applied to every memory cell 12 along an active row via a corresponding word line (WL) 28, a corresponding source line (CN) 30, and/or a corresponding carrier injection line (EP) 34. However, while the active operations may be performed on one or more selected memory cells 12 along the active row, one or more unselected memory cells 12 (e.g., corresponding to bit lines (EN<2>) and (EN<3>) 32) along the active row may experience a disturbance caused by the voltage potentials applied via the corresponding word line (WL) 28, the corresponding source line (CN) 30, and/or the corresponding carrier injection line (EP) 34 during the active operations. In order to reduce a disturbance experienced by the one or more unselected memory cells 12 (e.g., corresponding to bit lines (EN<2>) and (EN<3>) 32) along the active row, a masking operation may be performed on the one or more unselected memory cells 12.

In an exemplary embodiment, during a masking operation, a voltage potential may be applied to the one or more unselected memory cells 12 on an active row via corresponding bit lines (EN<2>) and (EN<3>) 32. The voltage potential applied via the corresponding bit lines (EN<2>) and (EN<3>) 32 to the one or more unselected memory cells 12 on the active row may be raised to a predetermined voltage potential. In an exemplary embodiment, the voltage potential applied to the corresponding bit lines (EN<2>) and (EN<3>) 32 associated with the one or more unselected memory cells 12 along the active row may be 1.1V in order to reduce a disturbance caused by the other voltage potentials applied during the active operations.

Referring to FIGS. 7A and 7B, there are shown a schematic representation and control signal voltage waveforms for performing a write logic high (e.g., binary “1” data state) operation on a memory cell in accordance with an embodiment of the present disclosure. The write logic high (e.g., binary “1” data state) operation may involve control signals

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that are configured to perform a write logic high (e.g., binary “1” data state) operation to one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. For example, the write logic high (e.g., binary “1” data state) operation may be performed on one or more selected rows of the memory cell array 20 or the entire memory cell array 20.

In an exemplary embodiment, during the write logic high (e.g., binary “1” data state) operation, a voltage potential applied to the N+ region 120 of a selected memory cell 12 via a corresponding bit line (EN) 32 may be maintained at 0V, a voltage potential applied to the P+ region 126 of the selected memory cell 12 via a corresponding carrier injection line (EP) 34 may be maintained at 0.7V, and a voltage potential applied to the word line (WL) 28 (e.g., capacitively coupled to the P- region 122) may be raised to -0.5V from -1.0V. Simultaneously to or subsequent to raising a voltage potential applied to the word line (WL) 28, a voltage potential applied to the source line (CN) 30 may be lowered to 0V from 0.7V.

Under such biasing, the junction between the N+ region 120 and the P- region 122 may be reverse biased and the junction between the P+ region 126 and the N+ region 124 may become forward biased. A logic high (e.g., binary “1” data state) may be written to the P- region 122 (e.g., majority charge carriers injected into the P- region 122 from the P+ region 126 via the N+ region 124) via the forward biased junction between the P+ region 126 and the N+ region 124. As more majority charge carriers accumulate in the P- region 122, the voltage potential at the P- region 122 may increase to approximately 0.7V to 1.0V above the voltage potential at the N+ region 124. A sufficient amount of majority charge carriers may be injected into the P- region 122 to represent that a logic high (e.g., binary “1” data state) is stored in the memory cell 12.

Referring to FIGS. 8A and 8B, there are shown a schematic representation and control signal voltage waveforms for performing a write logic high (e.g., binary “1” data state) operation on a memory cell in accordance with an alternative embodiment of the present disclosure. The write logic high (e.g., binary “1” data state) operation may involve control signals that are configured to perform a write logic high (e.g., binary “1” data state) operation on one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. For example, the write logic high (e.g., binary “1” data state) operation may be performed on one or more selected rows of the memory cell array 20 or the entire memory cell array 20.

In an exemplary embodiment, during the write logic high (e.g., binary “1” data state) operation, a voltage potential applied to the N+ region 120 of a selected memory cell 12 via a corresponding bit line (EN) 32 may be maintained at 0V, a voltage potential applied to the P+ region 126 of the selected memory cell 12 via a corresponding carrier injection line (EP) 34 may be maintained at 1.0V, and a voltage potential applied to the word line (WL) 28 (e.g., capacitively coupled to the P- region 122) may be raised to -0.7V from -1.0V. Simultaneously to or subsequent to raising a voltage potential applied to the word line (WL) 28, a voltage potential applied to the source line (CN) 30 may be lowered to 0.3V from 1.0V.

Under such biasing, the junction between the N+ region 120 and the P- region 122 may be reverse biased and the junction between the P+ region 126 and the N+ region 124 may become forward biased. A logic high (e.g., binary “1” data state) may be written to the P- region 122 (e.g., majority charge carriers injected into the P- region 122 from

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the P+ region 126 via the N+ region 124) via the forward biased junction between the P+ region 126 and the N+ region 124. As more majority charge carriers accumulate in the P- region 122, the voltage potential at the P- region 122 may increase to approximately 0.7V to 1.0V above the voltage potential at the N+ region 124. A sufficient amount of majority charge carriers may be injected into the P- region 122 to represent that a logic high (e.g., binary "1" data state) is stored in the memory cell 12.

Referring to FIGS. 9A and 9B, there are shown a schematic representation and control signal voltage waveforms for performing a write logic low (e.g., binary "0" data state) operation on a memory cell in accordance with an embodiment of the present disclosure. For example, a write logic low (e.g., binary "0" data state) operation may involve control signals that are configured to perform one or more write operations on one or more selected memory cells 12. For example, the write logic low (e.g., binary "0" data state) operation may be performed on one or more selected memory cells 12 after a write logic high (e.g., binary "1" data state) operation in order to deplete majority charge carriers that may have accumulated in the P- regions 122 of the one or more selected memory cells 12.

In an exemplary embodiment, a voltage potential applied to the N+ region 120 via the bit line (EN("0")) 32 may be maintained at 0V in order to perform the write logic low (e.g., binary "0" data state) operation. A voltage potential applied to the N+ region 124 via the source line (CN) 30 may be raised to 1.1V from 0V in order to perform a write logic low (e.g., binary "0" data state) operation. Subsequent to or simultaneously to raising the voltage potential applied to the N+ region 124 via the source line (CN) 30, a voltage potential applied to the word line (WL) 28 may be raised to approximately 0.5V from -1.0V.

Under such biasing, the junction between the N+ region 120 and the P- region 122 may become forward biased. The junction between the N+ region 124 and the P- region 122 may become reverse biased or become weakly forward biased (e.g., above a reverse bias voltage and below a forward bias threshold voltage, or a voltage potential at a p-diffusion region in the P- region 122 may be higher than a voltage potential at an n-diffusion region in the N+ region 124). Majority charge carriers that may have accumulated in the P- region 122 during a write logic high (e.g., binary "1" data state) operation may be removed via the forward biased junction between the N+ region 120 and the P- region 122. After removing the majority charge carriers from the P- region 122, a logic low (e.g., binary "0" data state) may be written to the memory cell 12.

In order to maintain a logic high (e.g., binary "1" data state) in one or more unselected memory cells 12 during the write logic low (e.g., binary "0" data state) operation, a masking operation may be performed on the one or more unselected memory cells 12. For example, a voltage potential applied to the N+ region 120 via a bit line (EN("1")) 32 of the one or more unselected memory cells 12 may be raised to 1.1V from 0.7V or higher (e.g., 1.2V) in order to prevent the depletion of majority charge carriers accumulated in the P- region 122. Under such biasing, the junction between the N+ region 120 and the P- region 122 may not be forward biased and the junction between the P- region 122 and the N+ region 124 may not be forward biased in order to prevent the depletion of majority charge carriers accumulated in the P- region 122 so as to allow the logic high (e.g., binary "1" data state) to be maintained in the memory cell 12.

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Referring to FIGS. 10A and 10B, there are shown a schematic representation and control signal voltage waveforms for performing a write logic low (e.g., binary "0" data state) operation on a memory cell in accordance with an alternative embodiment of the present disclosure. For example, a write logic low (e.g., binary "0" data state) operation may involve control signals that are configured to perform one or more write operations on one or more selected memory cells 12. For example, the write logic low (e.g., binary "0" data state) operation may be performed on one or more selected memory cells 12 after a write logic high (e.g., binary "1" data state) operation in order to deplete majority charge carriers that may have accumulated in the P- regions 122 of the one or more selected memory cells 12.

In an exemplary embodiment, a voltage potential applied to the N+ region 120 via the bit line (EN("0")) 32 may be maintained at 0V in order to perform the write logic low (e.g., binary "0" data state) operation. A voltage potential applied to the N+ region 124 via the source line (CN) 30 may be maintained at 1.0V in order to perform a write logic low (e.g., binary "0" data state) operation. A voltage potential applied to the P+ region 126 via the carrier injection line (EP) 34 may be maintained at 1.0V. A voltage potential applied to the word line (WL) 28 may be raised to approximately 0.5V from -1.0V.

Under such biasing, the junction between the N+ region 120 and the P- region 122 may become forward biased. The junction between the N+ region 124 and the P- region 122 may become reverse biased or become weakly forward biased (e.g., above a reverse bias voltage and below a forward bias threshold voltage, or a voltage potential at a p-diffusion region in the P- region 122 may be higher than a voltage potential at an n-diffusion region in the N+ region 124). Majority charge carriers that may have accumulated in the P- region 122 during a write logic high (e.g., binary "1" data state) operation may be removed via the forward biased junction between the N+ region 120 and the P- region 122. After removing the majority charge carriers from the P- region 122, a logic low (e.g., binary "0" data state) may be written to the memory cell 12.

In order to maintain a logic high (e.g., binary "1" data state) in one or more unselected memory cells 12 during the write logic low (e.g., binary "0" data state) operation, a masking operation may be performed on the one or more unselected memory cells 12. For example, a voltage potential applied to the N+ region 120 via a bit line (EN("1")) 32 of the one or more unselected memory cells 12 may be raised to 1.0V from 0V or higher (e.g., 1.2V) in order to prevent the depletion of majority charge carriers accumulated in the P- region 122. Under such biasing, the junction between the N+ region 120 and the P- region 122 may not be forward biased and the junction between the P- region 122 and the N+ region 124 may not be forward biased in order to prevent the depletion of majority charge carriers accumulated in the P- region 122 so as to allow the logic high (e.g., binary "1" data state) to be maintained in the memory cell 12.

At this point it should be noted that providing a direct injection semiconductor memory device in accordance with the present disclosure as described above typically involves the processing of input data and the generation of output data to some extent. This input data processing and output data generation may be implemented in hardware or software. For example, specific electronic components may be employed in a direct injection semiconductor memory device or similar or related circuitry for implementing the functions associated with providing a direct injection semi-

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conductor memory device in accordance with the present disclosure as described above. Alternatively, one or more processors operating in accordance with instructions may implement the functions associated with providing a direct injection semiconductor memory device in accordance with the present disclosure as described above. If such is the case, it is within the scope of the present disclosure that such instructions may be stored on one or more processor readable media (e.g., a magnetic disk or other storage medium), or transmitted to one or more processors via one or more signals embodied in one or more carrier waves.

The present disclosure is not to be limited in scope by the specific embodiments described herein. Indeed, other various embodiments of and modifications to the present disclosure, in addition to those described herein, will be apparent to those of ordinary skill in the art from the foregoing description and accompanying drawings. Thus, such other embodiments and modifications are intended to fall within the scope of the present disclosure. Further, although the present disclosure has been described herein in the context of a particular implementation in a particular environment for a particular purpose, those of ordinary skill in the art will recognize that its usefulness is not limited thereto and that the present disclosure may be beneficially implemented in any number of environments for any number of purposes. Accordingly, the claims set forth below should be construed in view of the full breadth and spirit of the present disclosure as described herein.

The invention claimed is:

1. A direct injection semiconductor memory device comprising:

- a first region coupled to a bit line;
- a second region coupled to a source line;
- a body region spaced apart from and capacitively coupled to a word line, wherein the body region is electrically floating and disposed between the first region and the second region, wherein the first region, the body region, the second region are arranged in a sequential contiguous manner; and
- a substrate coupled to a carrier injection line, wherein the second region is disposed directly on the substrate, and wherein the body region is disposed directly on the second region opposite the substrate.

2. The direct injection semiconductor memory device of claim 1, wherein the first region and the second region have a common first doping polarity.

3. The direct injection semiconductor memory device of claim 2, wherein the first region and the second region are doped with donor impurities.

4. The direct injection semiconductor memory device of claim 2, wherein the first region and the second region are doped with acceptor impurities.

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5. The direct injection semiconductor memory device of claim 2, wherein the first region and the second region have different doping concentrations.

6. The direct injection semiconductor memory device of claim 2, wherein the body region and the substrate have a common second doping polarity.

7. The direct injection semiconductor memory device of claim 6, wherein the body region and the substrate are doped with donor impurities.

8. The direct injection semiconductor memory device of claim 6, wherein the body region and the substrate are doped with acceptor impurities.

9. The direct injection semiconductor memory device of claim 6, wherein the body region and the substrate have different doping concentrations.

10. The direct injection semiconductor memory device of claim 1, wherein the first region, the body region, and the second region form a bipolar transistor.

11. The direct injection semiconductor memory device of claim 10, wherein the bipolar transistor is an NPN transistor.

12. The direct injection semiconductor memory device of claim 10, wherein the bipolar transistor is a PNP transistor.

13. The direct injection semiconductor memory device of claim 1, wherein the second region and the substrate form a PN junction diode.

14. The direct injection semiconductor memory device of claim 1, wherein the first region, the body region, and the second region are formed in a sequential contiguous vertical structure substantially perpendicular to a plane formed by the substrate.

15. The direct injection semiconductor memory device of claim 1, wherein the word line is disposed on at least two opposing sides of the memory cell.

16. The direct injection semiconductor memory device of claim 1, wherein the source line and the bit line are disposed on opposite sides of the memory cell.

17. The direct injection semiconductor memory device of claim 1, wherein the source line is disposed on at least two opposing sides of the memory cell.

18. The direct injection semiconductor memory device of claim 1, wherein the second region is configured at least in part as a planar base region upon which the first region and the body region are formed in a sequential contiguous vertical structure substantially perpendicular to the planar base region.

19. The direct injection semiconductor memory device of claim 18, wherein the planar base region is formed directly on the substrate.

20. The direct injection semiconductor memory device of claim 18, wherein the planar base region is shared by at least one additional direct injection semiconductor memory device.

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